ADT7490

dBCool® Remote Thermal Monitor and Fan Controller with PECI Interface

The ADT7490 is a dBCool thermal monitor and multiple PWM fan controller for noise−sensitive or power−sensitive applications requiring active system cooling. The ADT7490 includes a local temperature sensor, two remote temperature sensors including series resistance cancellation, and monitors CPU temperature with a PECI interface. The ADT7490 can drive a fan using either a low or high frequency drive signal, and measure and control the speed of up to four fans so they operate at the lowest possible speed for minimum acoustic noise.

The automatic fan speed control loop optimizes fan speed for a given temperature using the PECI, remote, or local temperature information. The effectiveness of the system's thermal solution can be monitored using the $\overline{\text{THERM}}$ input. The ADT7490 also provides critical thermal protection to the system using the bidirectional $\overline{\text{THERM}}$/$\overline{\text{SMBALERT}}$ pin as an output to prevent system or component overheating.

Features

- Temperature Measurement
  - 1 Local On−Chip Temperature Sensor
  - 2 Remote Temperature Sensors
  - 3 Current External Temperature Sensors with Series Resistance Cancellation (SRC)
  - PECI Interface for CPU Thermal Information and Support of Up to 4 PECI Inputs on 1 Pin
- Fan Drive and Fan Speed Control
  - 3 High Frequency or Low Frequency PWM Outputs for Use with 3−Wire or 4−Wire Fans
  - 4 TACH Inputs to Measure Fan Speed
  - OS Independent Automatic Fan Speed Control Based on Thermal Information
  - Dynamic T_{MIN} Control Mode to Optimize System Acoustics
  - Default Startup at 100% PWM for All Fans for Robust Operation
- Bidirectional $\overline{\text{THERM}}$/$\overline{\text{SMBALERT}}$ Pin to Flag Out−of−Limit and Overtemperature Conditions
- GPIO Functionality to Support Extra Features
  - Can be Used for Loadline Setting for Voltage Regulation, LED Control, or Other Functions
- I_{MON} Monitoring for CPU Current and Power Information
- Footprint and Register Compatible with ADT7473/ADT7475/ ADT7476/ADT7476A Family of Fan Controllers
- SMBus Interface with Addressing Capability for Up to 3 Devices

Applications

- Personal Computers
- Servers

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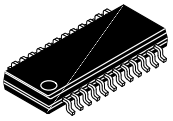
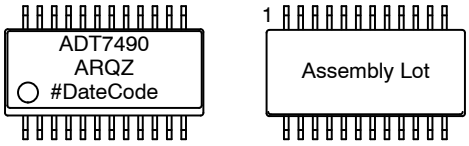
QSOP−24 NB
CASE 492B



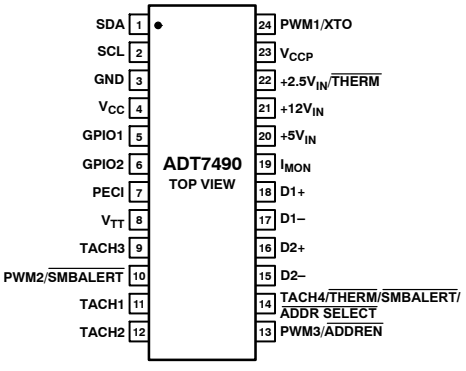
MARKING DIAGRAMS



TOP MARKING **BOTTOM MARKING**

= Pb−Free Package

PIN ASSIGNMENT



ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 74 of this data sheet.

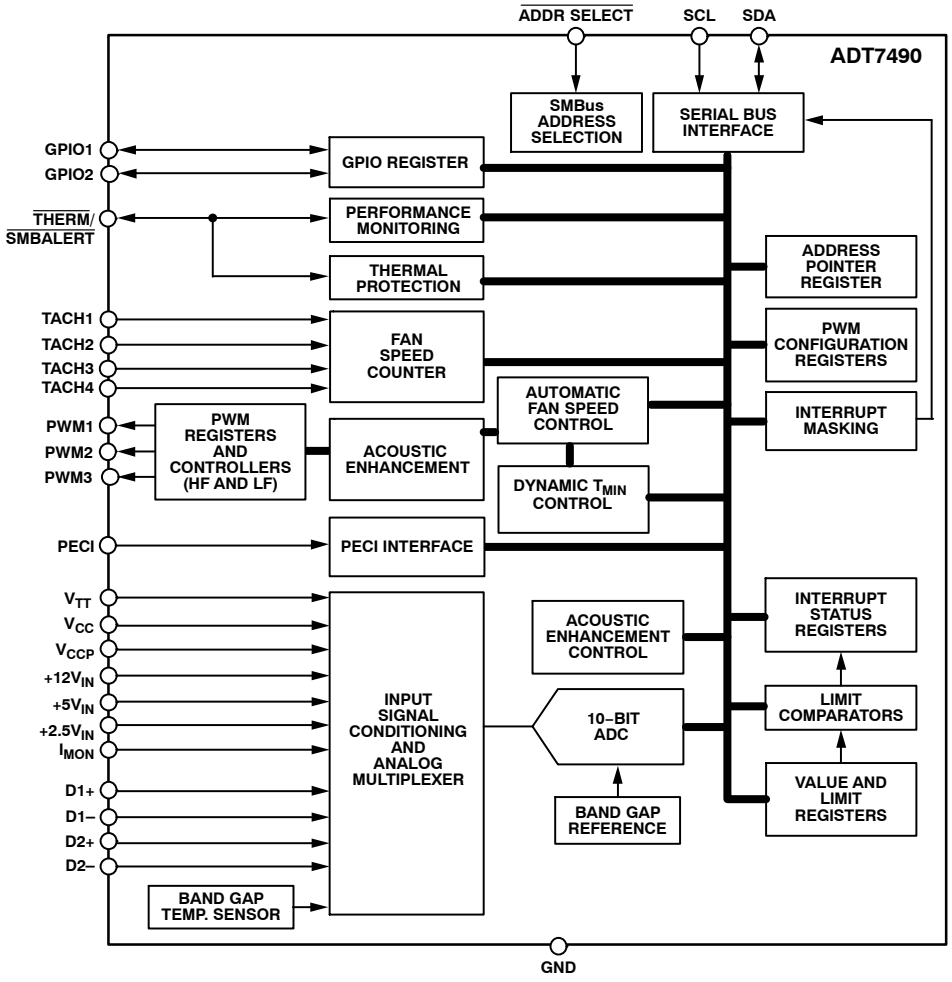


Figure 1. Functional Block Diagram

ABSOLUTE MAXIMUM RATINGS

Parameter	Rating	Unit
Positive Supply Voltage (V_{CC})	3.6	V
Maximum Voltage on +12 V_{IN} Pin	16	V
Maximum Voltage on +5 V_{IN} Pin	6.25	V
Maximum Voltage on All Open−Drain Outputs (excluding PWM pins)	3.6	V
Maximum Voltage on TACHx/PWMx Pins	+5.5	V
Voltage on Remaining Input or Output Pins	−0.3 to +4.2	V
Input Current at Any Pin	±5	mA
Package Input Current	±20	mA
Maximum Junction Temperature ($T_{J\ max}$)	150	°C
Storage Temperature Range	−65 to +150	°C
Lead Temperature, Soldering IR Reflow Peak Temperature Pb−Free Peak Temperature Lead Temperature (Soldering, 10 sec)	 220 260 300	°C
ESD Rating HBM FICDM	 2 0.5	kV

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

NOTE: This device is ESD sensitive. Use standard ESD precautions when handling.

THERMAL CHARACTERISTICS

Package Type	θ_{JA}	θ_{JC}	Unit
24−lead QSOP	122	31.25	°C/W

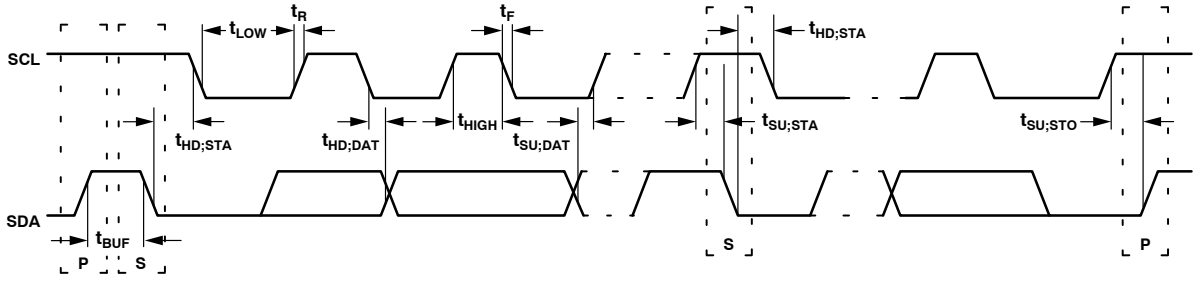


Figure 2. SMBus Bus Timing

ELECTRICAL CHARACTERISTICS $T_A = T_{MIN}$ to T_{MAX}, $V_{CC} = V_{MIN}$ to V_{MAX}, unless otherwise noted. (Note 1)

Parameter	Conditions	Min	Typ	Max	Unit
Power Supply					
Supply Voltage		3.0	3.3	3.6	V
Supply Current, I_{CC}	Interface inactive, ADC active		1.5	5.0	mA
Temperature−to−Digital Converter					
Local Sensor Accuracy Resolution	0°C ≤ T_A ≤ 85°C −40°C ≤ T_A ≤ +125°C		±0.5 0.25	±1.5 ±2.5	°C
Remote Diode Sensor Accuracy	0°C ≤ T_A ≤ 85°C −40°C ≤ T_A ≤ +125°C		±0.5 0.25	±1.5 ±2.5	°C
Remote Sensor Source Current	Mid level Low level High level		12 72 192		μA
Series Resistance Cancellation (Note 2)	The ADT7490 cancels up to 2 kΩ in series with the remote thermal sensor			1.5	kΩ
Analog−to−Digital Converter (Including MUX and Attentuators)					
Total Unadjusted Error (TUE)	For all channels: −40°C ≤ T_A ≤ +125°C For all other channels except +12 V_{IN}: 0°C ≤ T_A ≤ +125°C			±2 ±1.5	%
Differential Non−linearity (DNL)	8 bits			±1	LSB
Power Supply Sensitivity			±0.1		%/V
Conversion Times (Note 2) Voltage Inputs V_{TT} Voltage Input (Note 3) Local Temperature Remote Temperature	Averaging enabled, all channels excluding V_{TT} (Note) Averaging enabled Averaging enabled Averaging enabled Averaging enabled		 11 12 12 38	 13 14 14 43	ms
Total Monitoring Cycle Time	 Averaging disabled		169 19	193	ms
Input Resistance	For +12 V_{IN} channel For all other channels	150 70	200 100		kΩ
Fan RPM−to−Digital Converter					
Accuracy	0°C ≤ T_A ≤ 85°C −40°C ≤ T_A ≤ +125°C			±10 ±14	%
Full−Scale Count				65,535	
Nominal Input RPM	Fan count = 0xBFFF Fan count = 0x3FFF Fan count = 0x0438 Fan count = 0x021C		109 329 5000 10,000		RPM
Open−Drain Digital Outputs, PWM1 TO PWM3, XTO					
Current Sink, I_{OL}				8.0	mA
Output Low Voltage, V_{OL}	I_{OUT} = −8.0 mA			0.4	V
High Level Output Current, I_{OH}	$V_{OUT} = V_{CC}$		0.1	20	μA
Open−Drain Serial Data Bus Output (SDA)					
Output Low Voltage, V_{OL}	I_{OUT} = −4.0 mA			0.4	V
High Level Output Current, I_{OH}	$V_{OUT} = V_{CC}$		0.1	1.0	μA
SMBus Digital Inputs (SCL, SDA)					
Input High Voltage, V_{IH}		2.0			V
Input Low Voltage, V_{IL}				0.8	V
Hysteresis			500		mV

ELECTRICAL CHARACTERISTICS $T_A = T_{MIN}$ to T_{MAX}, $V_{CC} = V_{MIN}$ to V_{MAX}, unless otherwise noted. (Note 1)

Parameter	Conditions	Min	Typ	Max	Unit
Digital I/O (PECI Pin) (Note 2)					
V_{TT}, Supply Voltage		0.95		1.26	V
Input High Voltage , V_{IH}		0.55 x V_{TT} (Note 3)			V
Input Low Voltage, V_{IL}				0.5 x V_{TT} (Note 3)	V
Hysteresis (Note 2)	Hysteresis between input switching levels	0.1 x V_{TT} (Note 3)			mV
High Level Output Source Current, I_{SOURCE}	V_{OH} = 0.75 x V_{TT}			6.0	mA
Low Level Output Sink Current, I_{SINK}	V_{OL} = 0.25 x V_{TT}	0.5		1.0	mA
Signal Noise Immunity, V_{NOISE}	Noise glitches from 10 MHz to 100 MHz, width up to 50 ns	300			mV p−p
Digital Input Logic Levels (TACH1 to TACH3)					
Input High Voltage, V_{IH}	Maximum input voltage	2.0		5.5	V
Input Low Voltage, V_{IL}	Minimum input voltage	−0.3		0.8	V
Hysteresis			0.5		V p−p
Digital Input Logic Levels ($\overline{\text{THERM}}$)					
Input High Voltage, V_{IH}		0.75 x V_{CCP}			V
Input Low Voltage, V_{IL}				0.4	V
Digital Input Current					
Input High Current, I_{IH}	$V_{IN} = V_{CC}$		±1		μA
Input Low Current, I_{IL}	V_{IN} = 0		±1		μA
Input Capacitance, C_{IN}			5.0		pF
Serial Bus Timing (Note 2)	(See Figure 2)				
Clock Frequency, f_{SCLK}		10		400	kHz
Glitch Immunity, t_{SW}				50	ns
Bus Free Time, t_{BUF}		4.7			μs
SCL Low Time, t_{LOW}		4.7			μs
SCL High Time, t_{HIGH}		4.0		50	μs
SCL, SDA Rise Time, t_r				1000	ns
SCL, SDA Fall Time, t_f				300	μs
Data Setup Time, $t_{SU;DAT}$		250			ns
Detect Clock Low Timeout, $t_{TIMEOUT}$	Can be optionally disabled	15		35	ms

1. All voltages are measured with respect to GND, unless otherwise specified. Typical voltages are T_A = 25°C and represent a parametric norm. Logic inputs accept input high voltages up to V_{MAX}, even when the device is operating down to V_{MIN}. Timing specifications are tested at logic levels of V_{IL} = 0.8 V for a falling edge, and V_{IH} = 2.0 V for a rising edge.
2. Guaranteed by design, not production tested.
3. V_{TT} is the voltage input on Pin 8. The V_{TT} voltage is determined by the processor installed on the system.

PIN ASSIGNMENT

Pin No.	Mnemonic	Type	Description
1	SDA	Digital I/O	SMBus Bidirectional Serial Data. Open drain, requires SMBus pullup.
2	SCL	Digital Input	SMBus Serial Clock Input. Open drain, requires SMBus pullup.
3	GND	Ground	Ground Pin.
4	V_{CC}	Power Supply	3.3 V ± 10%.
5	GPIO1	Digital Input/Output	General−Purpose Open−Drain Digital Input/Output. Frequently used for switching load line resistors into VR load line circuitry or for switching LEDs using external FETs.
6	GPIO2	Digital Input/Output	General−Purpose Open−Drain Digital Input/Output. Frequently used for switching load line resistors into VR load line circuitry or for switching LEDs using external FETs.
7	PECI	Digital Input/Output	PECI Input to Report CPU Thermal Information. PECI voltage level is referenced on the V_{TT} input.
8	V_{TT}	Analog Input	Voltage Reference for PECI. This is the supply voltage for the PECI interface and must be present to measure temperature over the PECI interface. This voltage is also monitored and presented in Register 0x1E.
9	TACH3	Digital Input	Fan Tachometer Input to Measure Speed of Fan 3 (Open−Drain Digital Input).
10	PWM2/$\overline{\text{SMBALERT}}$	Digital Output	Pulse−Width Modulated Output to Control Fan 2 Speed. Open drain requires 10 kΩ typical pullup. Digital Output (Open Drain). This pin can be reconfigured as an $\overline{\text{SMBALERT}}$ interrupt output to signal out−of−limit conditions.
11	TACH1	Digital Input	Fan Tachometer Input to Measure Speed Of Fan 1 (Open−Drain Digital Input).
12	TACH2	Digital Input	Fan Tachometer Input To Measure Speed Of Fan 2 (Open−Drain Digital Input).
13	PWM3/ $\overline{\text{ADDREN}}$	Digital Output	Pulse−Width Modulated Output to Control Fan 3 Speed. Open drain requires 10 kΩ typical pullup. If pulled low on powerup, the ADT7490 enters address select mode, and the state of Pin 14 ($\overline{\text{ADDR SELECT}}$) determines the ADT7490 slave address.
14	TACH4/$\overline{\text{THERM}}$/ $\overline{\text{SMBALERT}}$/ $\overline{\text{ADDR SELECT}}$	Digital Input/Output	Fan Tachometer Input to Measure Speed of Fan 4 (Open−Drain Digital Input). May be reconfigured as a bidirectional $\overline{\text{THERM}}$ pin. Can be connected to the $\overline{\text{PROCHOT}}$ output of the processor, to time and monitor $\overline{\text{PROCHOT}}$ assertions. Can be used as an output to signal overtemperature conditions or for clock modulation purposes. Active Low Digital Output. The $\overline{\text{SMBALERT}}$ pin is used to signal out−of−limit comparisons of temperature, voltage, and fan speed. This is compatible with SMBus alert. Can also be used at device powerup to assign SMBus address.
15	D2−	Analog Input	Negative Connection for Remote Temperature Sensor 2.
16	D2+	Analog Input	Positive Connection to Remote Temperature Sensor 2.
17	D1−	Analog Input	Negative Connection for Remote Temperature Sensor 1.
18	D1+	Analog Input	Positive Connection to Remote Temperature Sensor 1.
19	I_{MON}	Analog Input	Monitors Current Output of Analog Devices ADP319x family of VRD10/VRD11 controllers.
20	+5 V_{IN}	Analog Input	Monitors 5.0 V Supply Using Internal Resistor Dividers.
21	+12 V_{IN}	Analog Input	Monitors 12 V Supply Using Internal Resistor Dividers.
22	+2.5 V_{IN}/$\overline{\text{THERM}}$	Analog Input	Monitors 2.5 V Supply Using Internal Resistor Dividers. Alternatively, this pin can be reconfigured as a bidirectional $\overline{\text{THERM}}$ pin. Can be connected to the $\overline{\text{PROCHOT}}$ output of the processor to time and monitor $\overline{\text{PROCHOT}}$ assertions. Can be used as an output to signal overtemperature conditions or for clock modulation purposes.
23	V_{CCP}	Analog Input	Monitors CPU V_{CC} Voltage (to maximum of 3.0 V). All voltage inputs can have their resistor dividers removed allowing for full−scale input of 2.25 V of the ADC channel.
24	PWM1/XTO	Digital Output	Pulse−Width Modulated Output to Control Fan 1 Speed. Open drain requires 10 kΩ typical pullup. Also functions as the output for the XNOR tree test enable mode.

Table 1. Comparison of ADT7490 and ADT7476A Configurations

Pin No.	ADT7490	ADT7476A
1	SDA	SDA
2	SCL	SCL
3	GND	GND
4	V_{CC}	V_{CC}
5	GPIO1	VID0/GPIO0
6	GPIO2	VID1/GPIO1
7	PECI	VID2/GPIO2
8	V_{TT}	VID3/GPIO3
9	TACH3	TACH3
10	PWM2/$\overline{\text{SMBALERT}}$	PWM2/$\overline{\text{SMBALERT}}$
11	TACH1	TACH1
12	TACH2	TACH2
13	PWM3/$\overline{\text{ADDREN}}$	PWM3/ $\overline{\text{ADDREN}}$
14	TACH4/$\overline{\text{THERM}}$/$\overline{\text{SMBALERT}}$/$\overline{\text{ADDR SELECT}}$	TACH4/$\overline{\text{THERM}}$/$\overline{\text{SMBALERT}}$/GPIO6/$\overline{\text{ADDR SELECT}}$
15	D2−	D2−
16	D2+	D2+
17	D1−	D1−
18	D1+	D1+
19	I_{MON}	VID4/GPIO4
20	+5 V_{IN}	+5 V_{IN}
21	+12 V_{IN}	+12 V_{IN}/VID5
22	+2.5 V_{IN}/ $\overline{\text{THERM}}$	+2.5 V_{IN}/ $\overline{\text{THERM}}$
23	V_{CCP}	V_{CCP}
24	PWM1/XTO	PWM1/XTO

TYPICAL CHARACTERISTICS

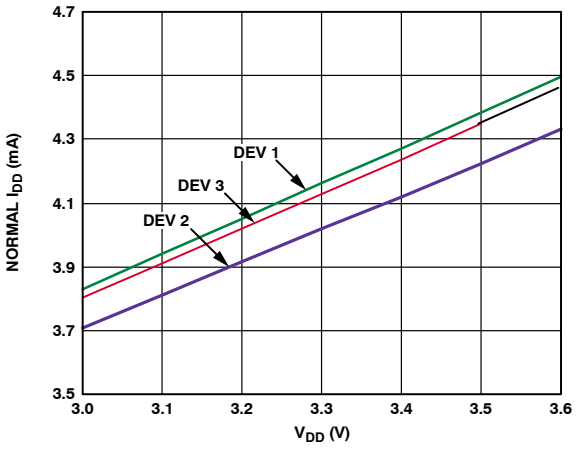


Figure 3. Supply Current vs. Supply Voltage

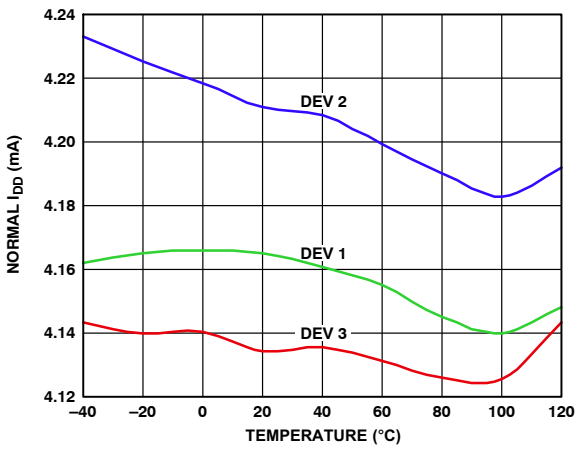


Figure 4. Supply Current vs. Temperature

TYPICAL CHARACTERISTICS

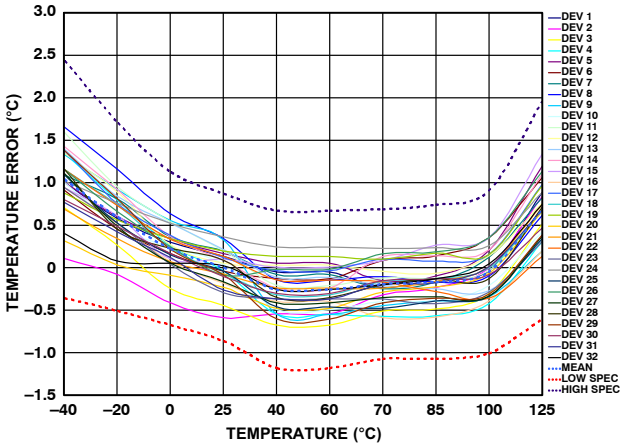


Figure 5. Local Temperature Sensor Error

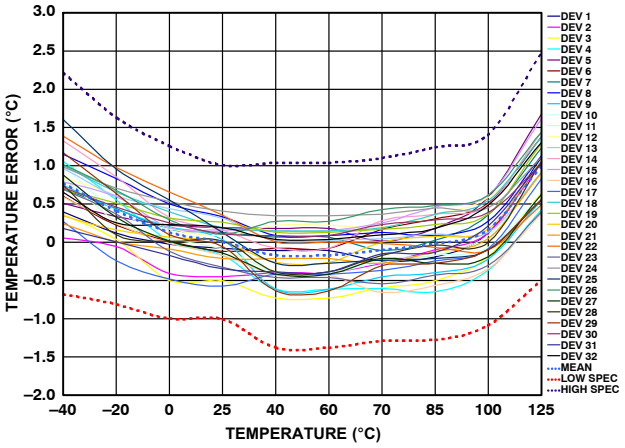


Figure 6. Remote 1 Temperature Sensor Error

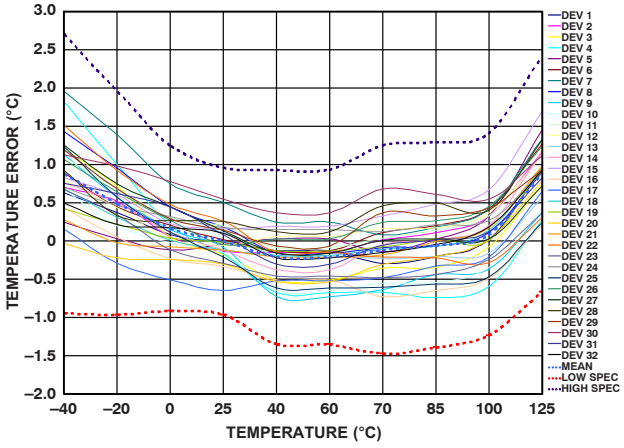


Figure 7. Remote 2 Temperature Sensor Error

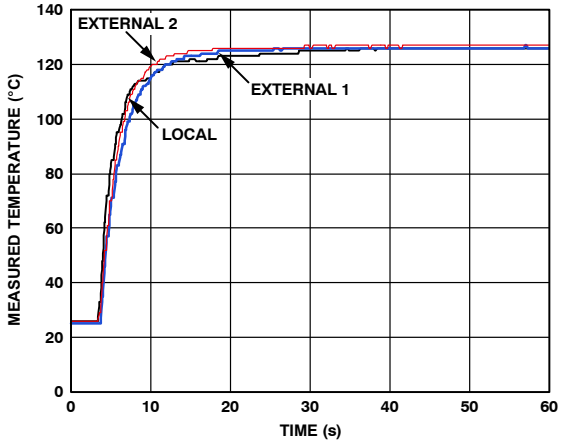


Figure 8. ADT7490 Response to Thermal Shock

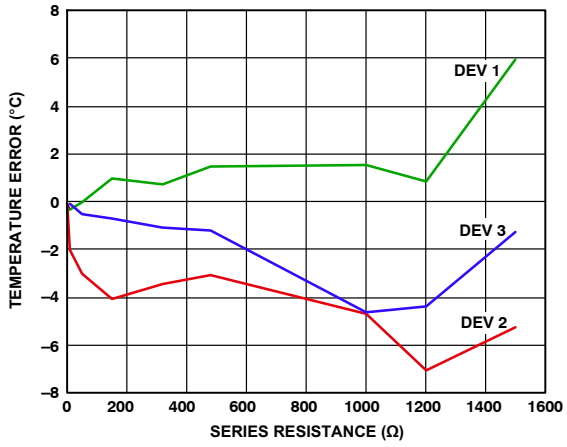


Figure 9. Temperature Error vs. Series Resistance

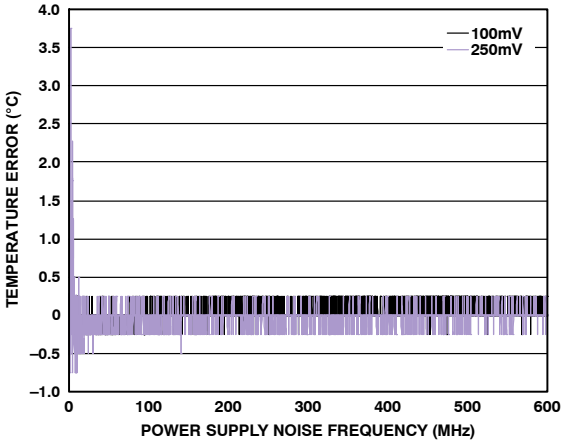


Figure 10. Local Temperature Error vs. Power Supply Noise Frequency

TYPICAL CHARACTERISTICS

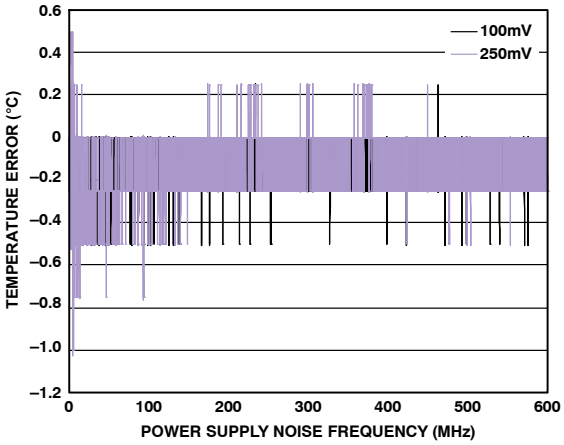


Figure 11. Remote Temperature Error vs. Power Supply Noise Frequency

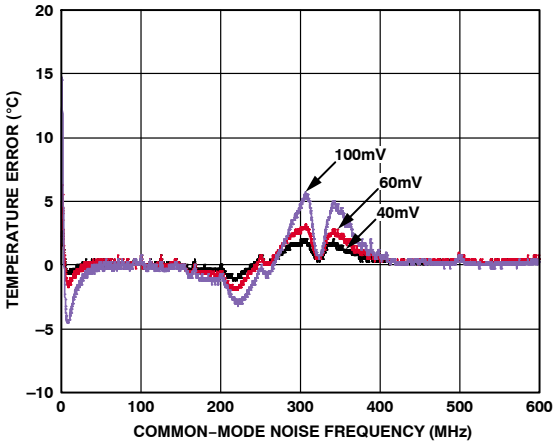


Figure 12. Temperature Error vs. Common−Mode Noise Frequency

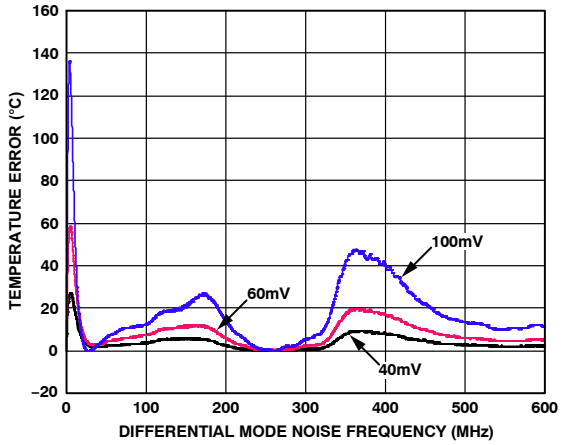


Figure 13. Temperature Error vs. Differential Mode Noise Frequency

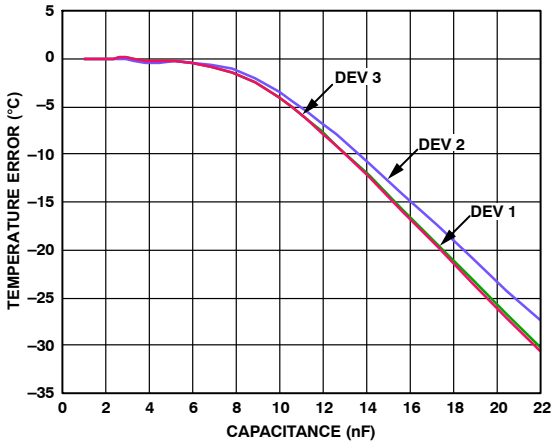


Figure 14. Temperature Error vs. Capacitance Between D+ and D−

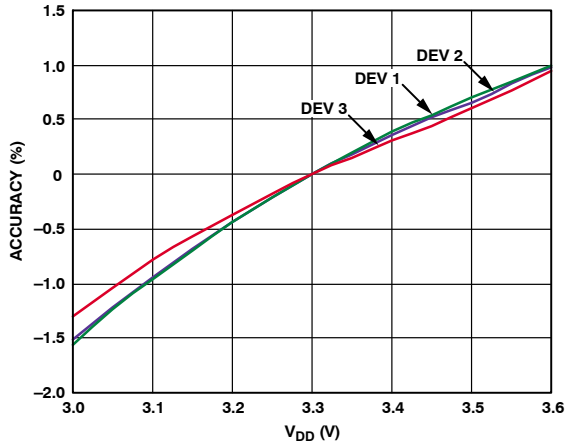


Figure 15. TACH Accuracy vs. Supply Voltage

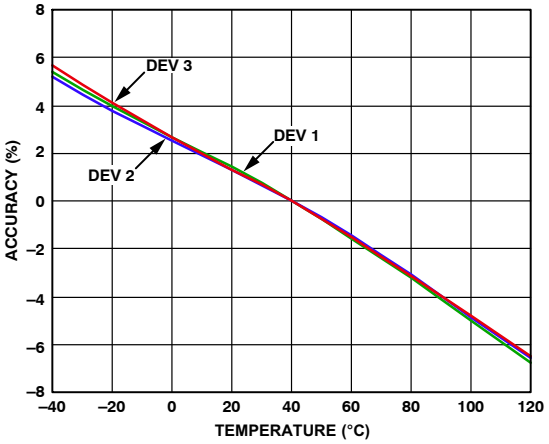


Figure 16. TACH Accuracy vs. Temperature

Theory of Operation

The ADT7490 is a complete thermal monitor and multiple fan controller for any system requiring thermal monitoring and cooling. The device communicates with the system via a serial system management bus. The serial bus controller has a serial data line for reading and writing addresses and data (Pin 1), and an input line for the serial clock (Pin 2). All control and programming functions for the ADT7490 are performed over the serial bus. In addition, Pin 14 can be reconfigured as an $\overline{\text{SMBALERT}}$ output to signal out−of−limit conditions.

Feature Comparisons Between the ADT7490 and ADT7476A

The ADT7490 is pin and register map compatible with the ADT7476A. The new or additional features are detailed in the following sections.

PECI Input

CPU thermal information is provided through the PECI input. The ADT7490 has PECI master capabilities and can read the CPU thermal information through the PECI interface. Each CPU address can have up to two PECI domains. The ADT7490 has the ability to record four PECI temperature readings corresponding to the four PECI addresses of 0x30 to 0x33. The hotter of the two domains at any given address is stored in the PECI value registers. A PECI reading is a negative value, in degrees Celsius, which represents the offset from the thermal control circuit (T_{CC}) activation temperature. PECI information is not converted to absolute temperature reading. PECI information is in a 16−bit twos complement value; however, the ADT7490 records the sign bit as well as the bits from 12:6 in the 16−bit PECI payload. See the Platform Environment Control Interface (PECI) Specification from Intel® for more details on the PECI data format. The PECI format is represented in Table 2.

Table 2. PECI Data Format

MSB Upper Nibble				MSB Lower Nibble			
S	x	x	x	x	x	x	x
Sign Bit				Integer value (0°C to 127°C)			

There are associated high and low limits for each PECI reading that can be programmed. The limit values take the same format as the PECI reading. Therefore, the programmed limits are not absolute temperatures but a relative offset in degrees Celsius from the T_{CC} activation temperature. An out−of−limit event is recorded as follows:

- High Limit > comparison performed
- Low Limit ≤ comparison performed

An out−of−limit event is recorded in the associated status register and can be used to assert the $\overline{\text{SMBALERT}}$ pin.

Temperature Data REPLACE Mode

The REPLACE mode is configured by setting Bit 4 of Register 0x36. In this mode, the data in the existing Remote 1 registers are replaced by PECI0 data and vice versa. This is a legacy mode that allows the thermal data from CPU1 to be stored in the same registers as in the ADT7476A. This reduces the software changes in systems transitioning from CPUs with thermal diodes to CPUs with a PECI interface. See the PECI Temperature Measurement section for more details.

Fan Control Using PECI Information

The CPU thermal information from PECI can be used in the existing automatic fan control algorithms. This temperature reading remains relative to T_{CC} activation temperature and the associated AFC control parameters are programmed in relative temperatures as opposed to absolute temperatures, and are in the same format as detailed in Table 2. $PECI_{MIN}$, T_{RANGE}, and $T_{CONTROL}$ are user defined.

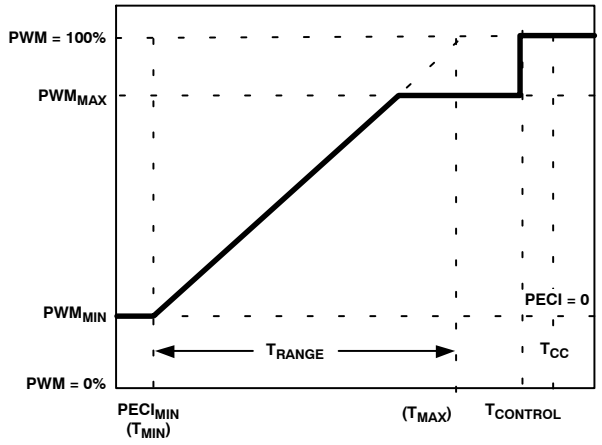


Figure 17. Overview of Automatic Fan Speed Control Using PECI Thermal Information

Dynamic TMIN Fan Control Mode

The automatic fan speed control incorporates a feature called dynamic T_{MIN} control. This intelligent fan control feature reduces the design effort required to program the automatic fan speed control loop and improves the system acoustics.

V_{TT} Input

The V_{TT} voltage is monitored on Pin 8. This voltage is also used as the reference voltage for the PECI interface. The V_{TT} voltage must be connected to the ADT7490 in order for the PECI interface to be operational.

I_{MON} Monitoring

The I_{MON} input on Pin 19 can be used to monitor the I_{MON} output of ON Semiconductor's VR10/VR11.1 controllers.

I_{MON} is a voltage representation of the CPU current. Using the I_{MON} value and the measured V_{CCP} value on Pin 23, the CPU power consumption can be calculated. See the appropriate Analog Devices flex mode data sheet for calculations. The I_{MON} information can be considered as an early indication of an increase in CPU temperature.

Startup Operation

At startup, the ADT7490 turns the fans on to 100% PWM. This allows the most robust operation at turn−on.

Serial Bus Interface

Control of the ADT7490 is carried out using the serial system management bus (SMBus). The ADT7490 is connected to this bus as a slave device, under the control of a master controller. The ADT7490 has a 7−bit serial bus address. When the device is powered up with Pin 13 (PWM3/$\overline{\text{ADDREN}}$) high, the ADT7490 has a default SMBus address of 0101110 or 0x2E. The read/write bit must be added to obtain the 8−bit address. If more than one ADT7490 is to be used in a system, each ADT7490 is placed in address select mode by strapping Pin 13 low on powerup. The logic state of Pin 14 then determines the device's SMBus address. The logic of these pins is sampled on powerup.

The device address is monitored from powerup but not latched until the first valid SMBus transaction, more precisely on the low−to−high transition at the beginning of the eighth SCL pulse, when the serial bus address byte matches the selected slave address. The selected slave address is chosen using the $\overline{\text{ADDREN}}$/ADDR SELECT pins. Any attempted changes in the address have no effect after this.

Table 3. Hard−wiring the ADT7490 SMBus Device Address

Pin 13 State	Pin 14 State	Address
0	Low (10 kΩ to GND)	0101100 (0x2C)
0	High (10 kΩ pullup)	0101101 (0x2D)
1	Don't care	0101110 (0x2E)

Data is sent over the serial bus in sequences of nine clock pulses: eight bits of data followed by an acknowledge bit from the slave device. Transitions on the data line must occur during the low period of the clock signal and remain stable during the high period, because a low−to−high transition when the clock is high may be interpreted as a stop signal. The number of data bytes that can be transmitted over the serial bus in a single read or write operation is limited only by what the master and slave devices can handle.

When all data bytes have been read or written, stop conditions are established. In write mode, the master pulls the data line high during the 10th clock pulse to assert a stop condition. In read mode, the master device overrides the acknowledge bit by pulling the data line high during the low period before the ninth clock pulse; this is known as no acknowledge. The master takes the data line low during the low period before the 10th clock pulse, and then high during the 10th clock pulse to assert a stop condition.

Any number of bytes of data can be transferred over the serial bus in one operation, but it is not possible to mix read and write in one operation because the type of operation is determined at the beginning and cannot subsequently be changed without starting a new operation.

In the ADT7490, write operations contain either one or two bytes, and read operations contain one byte. To write data to one of the device data registers or read data from it, the address pointer register must be set so that the correct data register is addressed. Then data can be written into that register or read from it. The first byte of a write operation always contains an address that is stored in the address pointer register. If data is to be written to the device, the write operation must contain a second data byte that is written to the register selected by the address pointer register.

This write operation is shown in Figure 18. The device address is sent over the bus, and then R/$\overline{\text{W}}$ is set to 0. This is followed by two data bytes. The first data byte is the address of the internal data register to be written to, which is stored in the address pointer register. The second data byte is the data to be written to the internal data register.

When reading data from a register, there are two possibilities:

- If the ADT7490 address pointer register value is unknown or not the desired value, it must first be set to the correct value before data can be read from the desired data register. This is done by performing a write to the ADT7490 as before, but only the data byte containing the register address is sent because no data is written to the register. This is shown in Figure 19.
  A read operation is then performed consisting of the serial bus address, R/$\overline{\text{W}}$ bit set to 1, followed by the data byte read from the data register. This is shown in Figure 20.
- If the address pointer register is known to be already at the desired address, data can be read from the corresponding data register without first writing to the address pointer register, as shown in Figure 20.

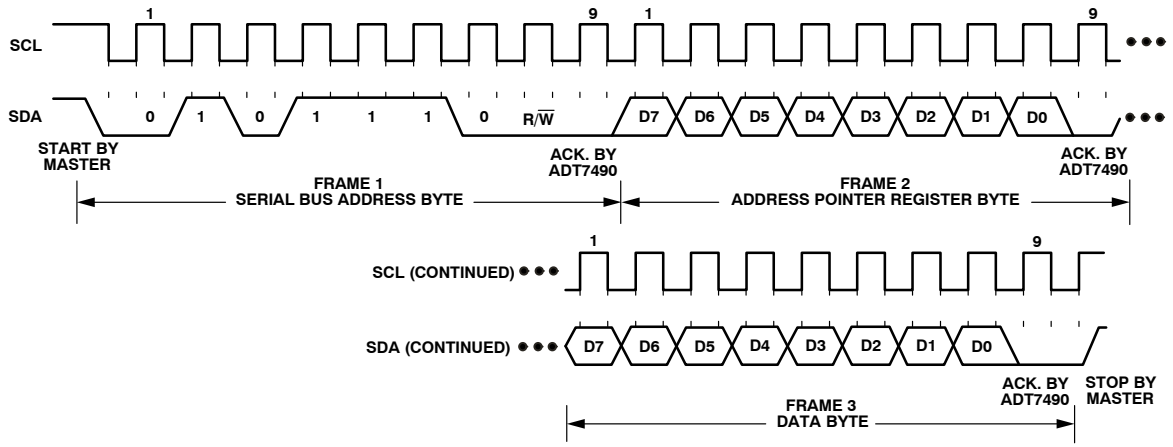


Figure 18. Writing a Register Address to the Address Pointer Register, then Writing Data to the Selected Register

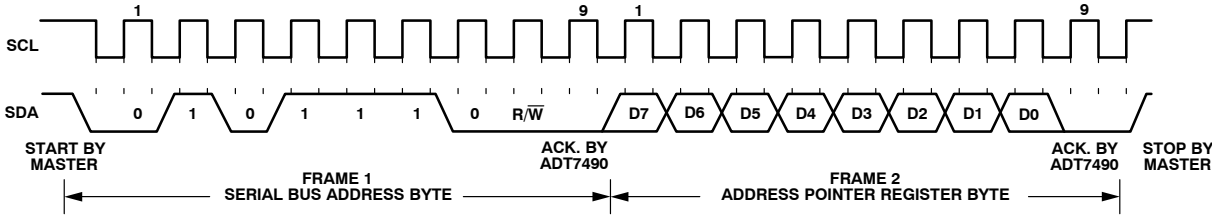


Figure 19. Writing to the Address Pointer Register Only

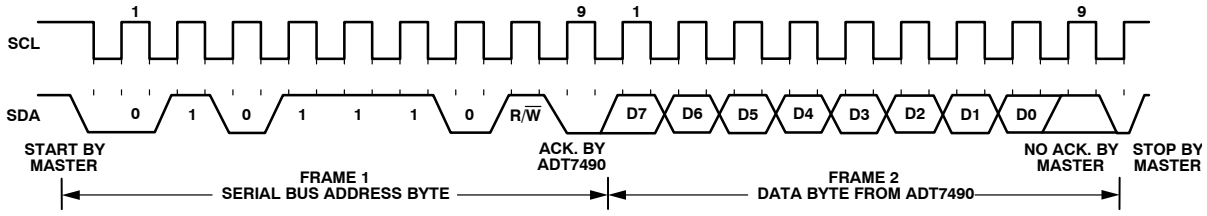


Figure 20. Reading Data from a Previously Selected Register

It is possible to read a data byte from a data register without first writing to the address pointer register if the address pointer register is already at the correct value. However, it is not possible to write data to a register without writing to the address pointer register because the first data byte of a write is always written to the address pointer register.

In addition to supporting the send byte and receive byte protocols, the ADT7490 also supports the read byte protocol (see System Management Bus Specifications Rev. 2 for more information; this document is available from the SMBus organization).

If several read or write operations must be performed in succession, the master can send a repeat start condition instead of a stop condition to begin a new operation.

Write Operations

The SMBus specification defines several protocols for different types of read and write operations. The ones used in the ADT7490 are discussed here. The following abbreviations are used in the diagrams:

- S: Start
- P: Stop
- R: Read
- $\overline{W}$: Write
- A: Acknowledge
- $\overline{A}$: No acknowledge

The ADT7490 uses the following SMBus write protocols.

Send Byte

In this operation, the master device sends a single command byte to a slave device, as follows:

1. The master device asserts a start condition on SDA.
2. The master sends the 7−bit slave address followed by the write bit (low).
3. The addressed slave device asserts ACK on SDA.

4. The master sends a command code.
5. The slave asserts ACK on SDA.
6. The master asserts a stop condition on SDA and the transaction ends.

For the ADT7490, the send byte protocol is used to write a register address to RAM for a subsequent single−byte read from the same address. This operation is illustrated in Figure 21.

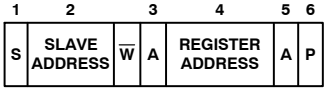


Figure 21. Setting a Register Address for Subsequent Read

If the master is required to read data from the register immediately after setting up the address, it can assert a repeat start condition immediately after the final ACK and carry out a single−byte read without asserting an intermediate stop condition.

Write Byte

In this operation, the master device sends a command byte and one data byte to the slave device, as follows:

1. The master device asserts a start condition on SDA.
2. The master sends the 7−bit slave address followed by the write bit (low).
3. The addressed slave device asserts ACK on SDA.
4. The master sends a command code.
5. The slave asserts ACK on SDA.
6. The master sends a data byte.
7. The slave asserts ACK on SDA.
8. The master asserts a stop condition on SDA, and the transaction ends.

The byte write operation is illustrated in Figure 22.

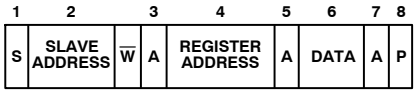


Figure 22. Single Byte Write to a Register

Read Operations

The ADT7490 uses the following SMBus read protocols.

Receive Byte

This operation is useful when repeatedly reading a single register. The register address must be previously set up. In this operation, the master device receives a single byte from a slave device, as follows:

1. The master device asserts a start condition on SDA.
2. The master sends the 7−bit slave address followed by the read bit (high).
3. The addressed slave device asserts ACK on SDA.
4. The master receives a data byte.
5. The master asserts NO ACK on SDA.
6. The master asserts a stop condition on SDA, and the transaction ends.

In the ADT7490, the receive byte protocol is used to read a single byte of data from a register whose address has previously been set by a send byte or write byte operation. This operation is illustrated in Figure 23.

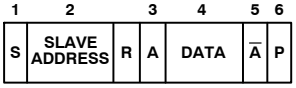


Figure 23. Single−Byte Read from a Register

Alert Response Address

Alert response address (ARA) is a feature of SMBus devices that allows an interrupting device to identify itself to the host when multiple devices exist on the same bus.

The $\overline{\text{SMBALERT}}$ output can be used as either an interrupt output or an $\overline{\text{SMBALERT}}$. One or more outputs can be connected to a common $\overline{\text{SMBALERT}}$ line connected to the master. If a device's $\overline{\text{SMBALERT}}$ line goes low, the following events occur:

1. $\overline{\text{SMBALERT}}$ is pulled low.
2. The master initiates a read operation and sends the alert response address (ARA = 0001 100). This is a general call address that must not be used as a specific device address.
3. The device whose $\overline{\text{SMBALERT}}$ output is low responds to the alert response address, and the master reads its device address. The address of the device is now known and can be interrogated in the usual way.
4. If more than one device's $\overline{\text{SMBALERT}}$ output is low, the one with the lowest device address has priority in accordance with normal SMBus arbitration.
5. Once the ADT7490 has responded to the alert response address, the master must read the status registers, and the $\overline{\text{SMBALERT}}$ is cleared only if the error condition is gone.

SMBus Timeout

The ADT7490 includes an SMBus timeout feature. If there is no SMBus activity for 35 ms, the ADT7490 assumes the bus is locked and releases the bus. This prevents the device from locking or holding the SMBus expecting data. Some SMBus controllers cannot work with the SMBus timeout feature, so it can be disabled.

Configuration Register 7 (Register 0x11)

Bit 4 (TODIS) = 0, SMBus timeout enabled (default)

Bit 4 (TODIS) = 1, SMBus timeout disabled

Voltage Measurement Input

The ADT7490 has six external voltage measurement channels. It can also measure its own supply voltage, V_{CC}.

Pin 20 to Pin 23 can measure 5.0 V, 12 V, and 2.5 V supplies, and the processor core voltage V_{CCP} (0 V to 3.0 V input). The 2.5 V input can be used to monitor a chipset supply voltage in computer systems. The V_{CC} supply voltage measurement is carried out through the V_{CC} pin (Pin 4). Pin 8 measures the V_{TT} voltage of the processor and

is the dedicated reference voltage for the PECI circuitry. The I_{MON} input on Pin 19 can be used to monitor the I_{MON} output of ON Semiconductor's VR11.1 controllers. I_{MON} is a voltage representation of the CPU current.

Analog−to−Digital Converter

All analog inputs are multiplexed into the on−chip, successive approximation, analog−to−digital converter. This ADC has a resolution of 10 bits. The basic input range is 0 V to 2.25 V, but the inputs have built−in attenuators to allow measurement of 2.5 V, 3.3 V, 5.0 V, 12 V, and the processor core voltage V_{CCP} without any external components. To allow the tolerance of these supply voltages, the ADC produces an output of 3/4 full scale (768 decimal or 0x300 hexadecimal) for the nominal input voltage, and therefore, has adequate headroom to cope with overvoltages.

Input Circuitry

The internal structure for the analog inputs is shown in Figure 24 . The input circuit consists of an input protection diode, an attenuator, plus a capacitor to form a first−order low−pass filter that gives input immunity to high frequency noise.

Voltage Measurement Registers

Register 0x1D, I_{MON} Reading = 0x00 default
Register 0x1E, V_{TT} Reading = 0x00 default
Register 0x20, +2.5 V_{IN} Reading = 0x00 default
Register 0x21, V_{CCP} Reading = 0x00 default
Register 0x22, V_{CC} Reading = 0x00 default
Register 0x23, +5 V_{IN} Reading = 0x00 default
Register 0x24, +12 V_{IN} Reading = 0x00 default

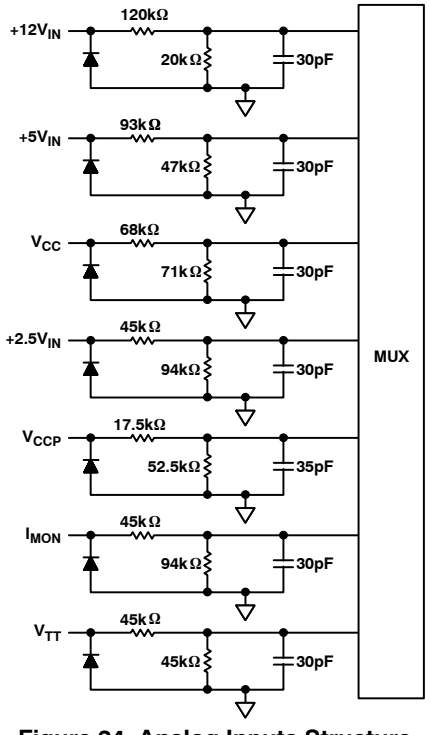


Figure 24. Analog Inputs Structure

Voltage Limit Registers

Associated with each voltage measurement channel is a high and low limit register. Exceeding the programmed high or low limit causes the appropriate status bit to be set. Exceeding either limit can also generate $\overline{\text{SMBALERT}}$ interrupts.

Register 0x85, I_{MON} Low Limit = 0x00 default

Register 0x87, I_{MON} High Limit = 0xFF default
Register 0x84, V_{TT} Low Limit = 0x00 default
Register 0x86, V_{TT} High Limit = 0xFF default
Register 0x44, +2.5 V_{IN} Low Limit = 0x00 default
Register 0x45, +2.5 V_{IN} High Limit = 0xFF default
Register 0x46, V_{CCP} Low Limit = 0x00 default
Register 0x47, V_{CCP} High Limit = 0xFF default
Register 0x48, V_{CC} Low Limit = 0x00 default
Register 0x49, V_{CC} High Limit = 0xFF default
Register 0x4A, +5 V_{IN} Low Limit = 0x00 default
Register 0x4B, +5 V_{IN} High Limit = 0xFF default
Register 0x4C, +12 V_{IN} Low Limit = 0x00 default
Register 0x4D, +12 V_{IN} High Limit = 0xFF default

When the ADC is running, it samples and converts a voltage input in 0.7 ms and averages 16 conversions to reduce noise; a measurement takes nominally 11 ms.

Extended Resolution Registers

Voltage measurements can be made with higher accuracy using the extended resolution registers (0x1F, 0x76, and 0x77). Whenever the extended resolution registers are read, the corresponding data in the voltage measurement registers (0x1D, 0x1E, and 0x20 to 0x24) is locked until their data is read. That is, if extended resolution is required, the extended resolution register must be read first, immediately followed by the appropriate voltage measurement register.

Additional ADC Functions for Voltage Measurements

A number of other functions are available on the ADT7490 to offer the system designer increased flexibility. The functions described in the following sections are enabled by setting the appropriate bit in Configuration Register 2.

Configuration Register 2 (Register 0x73)

Bit 4 (AVG) = 1, averaging off.

Bit 5 (ATTN) = 1, bypass input attenuators.

Bit 6 (CONV) = 1, single−channel convert mode.

Turn−Off Averaging

For each voltage/temperature measurement read from a value register, 16 readings have actually been made internally and the results averaged before being placed into the value register. When faster conversions are needed, setting Bit 4 (AVG) of Configuration Register 2 (0x73) turns averaging off. This effectively gives a reading that is 16 times faster, but the reading can be noisier. The default round−robin cycle time takes 146.5 ms.

Table 4. Conversion Time with Averaging Disabled

Channel	Measurement Time (ms)
Voltage Channels	0.7
Remote Temperature 1	7
Remote Temperature 2	7
Local Temperature	1.3

When Bit 7 (ExtraSlow) of Configuration Register 6 (0x10) is set, the default round−robin cycle time increases to 240 ms.

Bypass All Voltage Input Attenuators

Setting Bit 5 of Configuration Register 2 (0x73) removes the attenuation circuitry from the 2.5 V_{IN}, V_{CCP}, V_{CC}, 5 V_{IN}, and 12 V_{IN} inputs. This allows the user to directly connect external sensors or rescale the analog voltage measurement inputs for other applications. The input range of the ADC without the attenuators is 0 V to 2.25 V.

Bypass Individual Voltage Input Attenuators

Bits [7:4] of Configuration Register 4 (0x7D) can be used to bypass individual voltage channel attenuators.

Table 5. Bypassing Individual Voltage Input Attenuators

Configuration Register 4 (0x7D)	
Bit No.	**Channel Attenuated**
4	Bypass +2.5 V_{IN} attenuator
5	Bypass V_{CCP} attenuator
6	Bypass +5 V_{IN} attenuator
7	Bypass +12 V_{IN} attenuator

Single−Channel ADC Conversion

While single−channel mode is intended as a test mode that can be used to increase sampling times for a specific channel, therefore helping to analyze that channel's performance in greater detail, it can also have other applications.

Setting Bit 6 of Configuration Register 2 (0x73) places the ADT7490 into single−channel ADC conversion mode. In this mode, the ADT7490 can read a single voltage channel only. The selected voltage input is read every 0.7 ms. The appropriate ADC channel is selected by writing to Bits [7:4] of the TACH1 minimum high byte register (0x55).

Table 6. Programming Single−Channel ADC Mode

Bits [7:4], Register 0x55	**Channel Selected** (Note 1)
0000	+2.5 V_{IN}
0001	V_{CCP}
0010	V_{CC}
0011	+5 V_{IN}
0100	+12 V_{IN}
0101	Remote 1 temperature
0110	Local temperature
0111	Remote 2 temperature
1000	V_{TT}
1001	I_{MON}

1. In the process of configuring single-channel ADC conversion mode, the TACH1 minimum high byte is also changed, possibly trading off TACH1 minimum high byte functionality with single-channel mode functionality.

Table 7. 10−Bit ADC Output Code vs. V_{IN}

Input Voltage						ADC Output	
+12 V_{IN}	+5 V_{IN}	V_{CC} (3.3 V_{IN})	+2.5 V_{IN}	V_{CCP}	V_{TT}/I_{MON}	Decimal	Binary (10 Bits)
<0.0156	<0.0065	<0.0042	<0.0032	<0.00293	<0.00220	0	00000000 00
0.0156 to 0.0312	0.0065 to 0.0130	0.0042 to 0.0085	0.0032 to 0.0065	0.0293 to 0.0058	0.00220 to 0.00440	1	00000000 01
0.0312 to 0.0469	0.0130 to 0.0195	0.0085 to 0.0128	0.0065 to 0.0097	0.0058 to 0.0087	0.00440 to 0,00660	2	00000000 10
0.0469 to 0.0625	0.0195 to 0.0260	0.0128 to 0.0171	0.0097 to 0.0130	0.0087 to 0.0117	0,00660 to 0.00881	3	00000000 11
0.0625 to 0.0781	0.0260 to 0.0325	0.0171 to 0.0214	0.0130 to 0.0162	0.0117 to 0.0146	0.00881 to 0.01100	4	00000001 00
0.0781 to 0.0937	0.0325 to 0.0390	0.0214 to 0.0257	0.0162 to 0.0195	0.0146 to 0.0175	0.01100 to 0.01320	5	00000001 01
0.0937 to 0.1093	0.0390 to 0.0455	0.0257 to 0.0300	0.0195 to 0.0227	0.0175 to 0.0205	0.01320 to 0.01541	6	00000001 10
0.1093 to 0.1250	0.0455 to 0.0521	0.0300 to 0.0343	0.0227 to 0.0260	0.0205 to 0.0234	0.01541 to 0.01761	7	00000001 11
0.1250 to 0.14060	0.0521 to 0.0586	0.0343 to 0.0386	0.0260 to 0.0292	0.0234 to 0.0263	0.01761 to 0.01981	8	00000010 00
–	–	–	–	–	–	–	–
4.0000 to 4.0156	1.6675 to 1.6740	1.1000 to 1.1042	0.8325 to 0.8357	0.7500 to 0.7529	0.5636 to 0.5658	256 (1/4 scale)	01000000 00
–	–	–	–	–	–	–	–
8.0000 to 8.0156	3.3300 to 3.3415	2.2000–2.2042	1.6650 to 1.6682	1.5000 to 1.5029	1.1272 to 1.1294	512 (1/2 scale)	10000000 00
–	–	–	–	–	–	–	–
12.0000 to 12.0156	5.0025 to 5.0090	3.3000 to 3.3042	2.4975 to 2.5007	2.2500 to 2.2529	1.6809 to 1.6930	768 (3/4 scale)	11000000 00
–	–	–	–	–	–	–	–
15.8281 to 15.8437	6.5983 to 6.6048	4.3527 to 4.3570	3.2942 to 3.2974	2.9677 to 2.9707	2.2301 to 2.2323	1013	11111101 01
15.8437 to 15.8593	6.6048 to 6.6113	4.3570 to 4.3613	3.2974 to 3.3007	2.9707 to 2.9736	2.2323 to 2.2346	1014	11111101 10
15.8593 to 15.8750	6.6113 to 6.6178	4.3613 to 4.3656	3.3007 to 3.3039	2.9736 to 2.9765	2.2346 to 2.2368	1015	11111101 11
15.8750 to 15.8906	6.6178 to 6.6244	4.3656 to 4.3699	3.3039 to 3.3072	2.9765 to 2.9794	2.2368 to 2.23899	1016	11111110 00
15.8906 to 15.9062	6.6244 to 6.6309	4.3699 to 4.3742	3.3072 to 3.3104	2.9794 to 2.9824	2,23899 to 2.2412	1017	11111110 01
15.9062 to 15.9218	6.6309 to 6.6374	4.3742 to 4.3785	3.3104 to 3.3137	2.9824 to 2.9853	2.2412 to 2.2434	1018	11111110 10
15.9218 to 15.9375	6.6374 to 6.4390	4.3785 to 4.3828	3.3137 to 3.3169	2.9853 to 2.9882	2.2434 to 2.2456	1019	11111110 11
15.9375 to 15.9531	6.6439 to 6.6504	4.3828 to 4.3871	3.3169 to 3.3202	2.9882 to 2.9912	2.2456 to 2.2478	1020	11111111 00
15.9531 to 15.9687	6.6504 to 6.6569	4.3871 to 4.3914	3.3202 to 3.3234	2.9912 to 2.9941	2.2478 to 2.25	1021	11111111 01
15.9687 to 15.9843	6.6569 to 6.6634	4.3914 to 4.3957	3.3234 to 3.3267	2.9941 to 2.9970	2.25 to 2.2522	1022	11111111 10
>15.9843	>6.6634	>4.3957	>3.3267	>2.9970	>2.2522	1023	1111111111 1

Temperature Measurement

The ADT7490 has four temperature measurement channels: one local, two remote thermal diodes, and a PECI. The local and thermal diode readings are analog temperature measurements, whereas PECI is a digital temperature reading.

PECI Temperature Measurement

The PECI interface is a dedicated thermal interface. The CPU temperature measurement is carried out internally in the CPU. This information is digitized and transferred to the ADT7490 via the PECI interface. The ADT7490 is a PECI host device and therefore, polls the CPU for thermal information.

The PECI measurement differs from traditional thermal diode temperature measurements in that the measurement is a relative value instead of an absolute value. The PECI reading is a negative value that indicates how close the CPU temperature is from the thermal throttling or T_{CC} point of the CPU.

The ADT7490 records and uses the PECI measurement for fan control in its relative format. Therefore, care must be taken in programming the relevant limits and fan control parameters in the PECI format. Refer to the PECI Input section and Table 2 for further PECI information.

PECI monitoring is enabled on the ADT7490 by setting the PECI monitoring bit in Configuration Register 1 (Register 0x40, Bit 4). The ADT7490 can measure the temperature of up to four dual−core CPUs. The number of CPUs in the system that provide PECI information is set in Bits [7:6] of Register 0x88. Each CPU is distinguished by the PECI address. The number of domains, or domain count, per CPU address must also be programmed into the ADT7490. The ADT7490 reads the temperature of both domains per CPU, however, only the PECI value of the hottest domain is recorded in the PECI value register.

PECI0 domains: Register 0x36, Bit 3

PECI1 domains: Register 0x88, Bit 5

PECI2 domains: Register 0x88, Bit 4

PECI3 domains: Register 0x88, Bit 3

PECI Reading Registers

Register 0x33, PECI0: PECI reading from CPU Address 0x30

Register 0x1A, PECI1: PECI reading from CPU Address 0x31

Register 0x1B, PECI2: PECI reading from CPU Address 0x32

Register 0x1C, PECI3: PECI reading from CPU Address 0x33

PECI Limit Registers

Each PECI measurement shares the same high and low limits.

Register 0x34, PECI Low Limit = 0x81 default

Register 0x35, PECI High Limit = 0x00 default

PECI Offset Registers

Each PECI reading has a dedicated offset register to calibrate the PECI measurement and account for errors in the temperature reading. The LSBs add a 1°C offset to the temperature reading so that the 8−bit register effectively allows temperature offsets of up to ±128°C with a resolution of 1°C.

Register 0x94, PECI0 Offset

Register 0x95, PECI1 Offset

Register 0x96, PECI2 Offset

Register 0x97, PECI3 Offset

PECI Data Smoothing

The PECI smoothing interval is programmed in PECI Configuration Register 1 (0x36). Bits [2:0] of Register 0x36 set the duration over which the PECI data being read by the ADT7490 is averaged. These bits set the duration over which smoothing is carried out on the PECI data read. The refresh rate in the PECI value registers is the same as the smoothing interval programmed.

The smoothing interval is calculated using the following formula:

$$\text{Smoothing Interval} = \#\text{reads} \times \left(t_{BIT} \times 67 \times \#\text{CPU} + t_{IDLE}\right) \quad \text{(eq. 1)}$$

where:

#reads is the number of readings defined in Register 0x36, Bits [2:0].

t_{BIT} is the negotiated bit rate.

67 is the number of bits in each PECI reading.

#CPU is the number of CPUs providing PECI data (1 to 4).

t_{IDLE} = 14 μs, the delay between consecutive reads.

For example,

#reads = 4096

t_{BIT} = 1 μs (1 MHz speed)

#CPU = 1

Smoothing Interval = 331 ms = PECI reading refresh rate

PECI Error Codes

There are two different error conditions for PECI data, PECI data errors, and PECI bus communications errors. Table 8 describes the two different error conditions. If the ADT7490 reads an error code (0x8000 to 0x8003) from the CPU over the PECI interface, Bit 1 is set in Interrupt Status 3 register (0x43), indicating a data error. The value of the error code is not included in the PECI value averaging sum. This means that a value of 0x00 is added to the PECI sum when an error code is recorded. The error code is not reported in the appropriate PECI value register. If an invalid FCS is recorded by the ADT7490, Bit 2 is set in the Interrupt Status 3 register (0x43), indicating a communications error. An alert is generated on the $\overline{\text{SMBALERT}}$ pin when either or both of these status bits are asserted.

Table 8. PECI Error Indicators

PECI Data	Description	Action
0x8000 to 0x8003	PECI data error	Bit 1 of Register 0x43 is set to 1
Invalid FCS	PECI communications error	Bit 2 of Register 0x43 is set to 1

Each PECI channel also has an associated status bit to indicate if the PECI high or low limits have been exceeded. An alert is generated on the $\overline{\text{SMBALERT}}$ pin when these status bits are asserted.

Table 9. PECI Status Bits

Channel	Register	Bit
PECI0	0x43	0
PECI1	0x81	3
PECI2	0x81	4
PECI3	0x81	5

Temperature Data REPLACE Mode

The REPLACE mode is configured by setting Bit 4 of Register 0x36. In this mode, the data in the existing Remote 1 registers are replaced by PECI0 data. This is a legacy mode that allows the thermal data from CPU1 to be stored in the same registers as in the ADT7476A. This reduces the software changes in systems transitioning from CPUs with thermal diodes to CPUs with a PECI interface. However, note that even though the associated registers are swapped, the correct data format (PECI vs. absolute temperature, see Table 2) must be written to and interpreted from these registers.

Notes

In Table 10, registers listed under the Remote 1 Default column are in absolute temperature format by default and are in PECI format in REPLACE mode. Registers listed under the PECI0 Default column are in PECI format by default and in absolute temperature format in REPLACE mode.

Table 10. Replace Mode Temperature Registers

Register Name	Remote 1 Default	PECI0 Default
Value Register	Reg. 0x25	Reg. 0x33
Low Limit	Reg. 0x4E	Reg. 0x34
High Limit	Reg. 0x4F	Reg. 0x35
T_{MIN}	Reg. 0x67	Reg. 0x3B
T_{RANGE}	Reg. 0x5F, Bits [7:4]	Reg. 0x3C, Bits [7:4]
Enhanced Acoustics	Reg. 0x62, Bits [2:0]	Reg. 0x3C, Bits [2:0]
Enhanced Acoustics Enable	Reg. 0x62, Bit 3	Reg. 0x3C, Bit 3
$\overline{\text{THERM}}$ $T_{CONTROL}$	Reg. 0x6A	Reg. 0x3D
T_{MIN} Hysteresis	Reg. 0x6D, Bits [7:4] Reg. 0x6D, Bits [3:0] (Note 1)	Reg. 0x6E, Bits [3:0] Reg. 0x6E, Bits [7:4] (Note 1)
Temperature offset	Reg. 0x70	Reg. 0x94
Operating Point for Dynamic T_{MIN}	Reg. 0x8B	Reg. 0x8A

1. In REPLACE mode, the Remote 2 and local temperature hysteresis values are swapped.

In REPLACE mode, the temperature zone controlling the relevant PWM output are also swapped from Remote 1 to PECI0. The swap of control only occurs if the default behavior setting for Register 0x5C Bits [7:5], Register 0x5D Bits [7:5] or Register 0x5E Bits [7:5] is 000.

Local Temperature Measurement

The ADT7490 contains an on−chip band gap temperature sensor whose output is digitized by the on−chip 10−bit ADC. The 8−bit MSB temperature data is stored in the local temperature register (Address 0x26). Because both positive and negative temperatures can be measured, the temperature data is stored in Offset 64 format or twos complement format, as shown in Table 11 and Table 12. Theoretically, the temperature sensor and ADC can measure temperatures from −128°C to +127°C (or −64°C to +191°C in the extended temperature range) with a resolution of 0.25°C. However, this exceeds the operating temperature range of the device, so local temperature measurements outside the ADT7490 operating temperature range are not possible.

Table 11. Twos Complement Temperature Data Format

Temperature	Digital Output (10−Bit) (Note 1)
−128°C	1000 0000 **00** (diode fault)
−63°C	1100 0001 **00**
−50°C	1100 1110 **00**
−25°C	1110 0111 **00**
−10°C	1111 0110 **00**
0°C	0000 0000 **00**
10.25°C	0000 1010 **01**
25.5°C	0001 1001 **10**
50.75°C	0011 0010 **11**
75°C	0100 1011 **00**
100°C	0110 0100 **00**
125°C	0111 1101 **00**
127°C	0111 1111 **00**

1. Bold numbers denote 2 LSBs of measurement in the Extended Resolution 2 register (Register 0x77) with 0.25°C resolution.

Table 12. Offset 64 Data Format

Temperature	Digital Output (10−Bit) (Note 1)
−64°C	0000 0000 **00** (diode fault)
−63°C	0000 0001 **00**
−1°C	0011 1111 **00**
0°C	0100 0000 **00**
1°C	0100 0001 **00**
10°C	0100 1010 **00**
25°C	0101 1001 **00**
50°C	0111 0010 **00**
75°C	1000 1001 **00**
100°C	1010 0100 **00**
125°C	1011 1101 **00**
191°C	1111 1111 **00**

1. Bold numbers denote 2 LSBs of measurement in the Extended Resolution 2 register (Register 0x77) with 0.25°C resolution.

Thermal Diode Temperature Measurement Method

A simple method of measuring temperature is to exploit the negative temperature coefficient of a diode, measuring the base−emitter voltage (V_{BE}) of a transistor operated at constant current. Unfortunately, this technique requires calibration to null out the effect of the absolute value of V_{BE}, which varies from device to device.

The technique used in the ADT7490 is to measure the change in V_{BE} when the device is operated at three different currents. Previous devices have used only two operating currents, but the use of a third current allows automatic cancellation of resistances in series with the external temperature sensor.

Figure 28 shows the input signal conditioning used to measure the output of an external temperature sensor. This figure shows the external sensor as a substrate transistor, but it could equally be a discrete transistor, such as a 2N3904/2N3906.

If a discrete transistor is used, the collector is not grounded and should be linked to the base. If a PNP transistor is used, the base is connected to the D− input and the emitter to the D+ input. If an NPN transistor is used, the emitter is connected to the D− input and the base to the D+ input. Figure 25 and Figure 26 show how to connect the ADT7490 to an NPN or PNP transistor for temperature measurement.

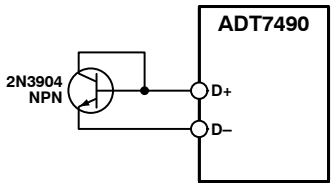


Figure 25. Measuring Temperature Using an NPN Transistor

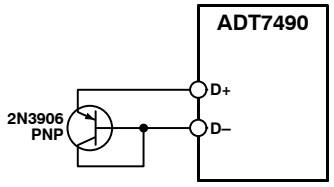


Figure 26. Measuring Temperature Using a PNP Transistor

To prevent ground noise from interfering with the measurement, the more negative terminal of the sensor is not referenced to ground, but is biased above ground by an internal diode at the D− input. C1 can optionally be added as a noise filter (recommended maximum value of 1000 pF). However, a better option in noisy environments is to add a filter, as described in the section.

Remote Temperature Measurement

The ADT7490 can measure the temperature of two remote diode sensors or diode−connected transistors connected to Pin 10 and Pin 11, or Pin 12 and Pin 13.

The forward voltage of a diode or diode−connected transistor operated at a constant current exhibits a negative temperature coefficient of about −2 mV/°C. Unfortunately, the absolute value of V_{BE} varies from device to device, and individual calibration is required to null this out. Therefore, the technique is unsuitable for mass production. The technique used in the ADT7490 is to measure the change in V_{BE} when the device is operated at three different currents. This is given by:

$$\Delta V_{BE} = \frac{KT}{q} \times \ln(N) \qquad \text{(eq. 2)}$$

where:

k is the Boltzmann constant.
q is the charge on the carrier.
T is the absolute temperature in Kelvin.
N is the ratio of the two currents.

To measure ΔV_{BE}, the operating current through the sensor is switched among three related currents. N1 x I and N2 x I are different multiples of the current I, as shown in Figure 27. The currents through the temperature diode are

switched between I and N1 x I, giving ΔV_{BE1}, and then between I and N2 x I, giving ΔV_{BE2}. The temperature can then be calculated using the two ΔV_{BE} measurements. This method can also cancel the effect of any series resistance on the temperature measurement.

The resulting ΔV_{BE} waveforms are passed through a 65 kHz low−pass filter to remove noise and then to a chopper−stabilized amplifier. This amplifies and rectifies the waveform to produce a dc voltage proportional to ΔV_{BE}. The ADC digitizes this voltage, and a temperature measurement is produced. To reduce the effects of noise, digital filtering is performed by averaging the results of 16 measurement cycles.

The results of remote temperature measurements are stored in 10−bit, twos complement format, as listed in Table 11. The extra resolution for the temperature measurements is held in the Extended Resolution Register 2 (0x77). This gives temperature readings with a resolution of 0.25°C.

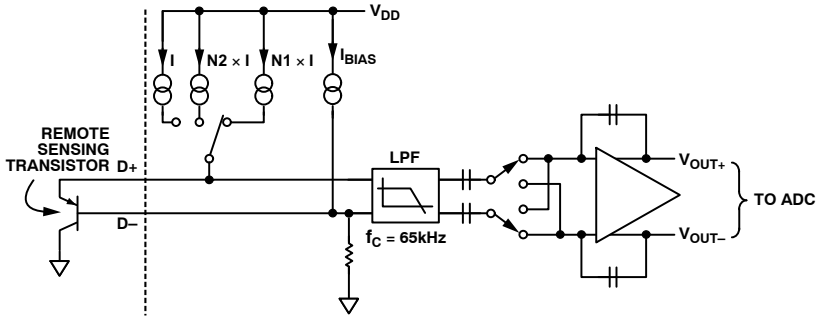


Figure 27. Signal Conditioning for Remote Diode Temperature Sensors

Series Resistance Cancellation

Parasitic resistance to the ADT7490 D+ and D− inputs (seen in series with the remote diode) is caused by a variety of factors, including PCB track resistance and track length. This series resistance appears as a temperature offset in the remote sensor's temperature measurement. This error typically causes a 0.5°C offset per ohm of parasitic resistance in series with the remote diode.

The ADT7490 automatically cancels out the effect of this series resistance on the temperature reading, giving a more accurate result without the need for user characterization of this resistance. The ADT7490 is designed to automatically cancel, typically up to 1.5 kΩ of resistance. By using an advanced temperature measurement method, this is transparent to the user. This feature allows resistances to be added to the sensor path to produce a filter, allowing the part to be used in noisy environments.

Noise Filtering

For temperature sensors operating in noisy environments, previous practice was to place a capacitor across the D+ pin and the D− pin to help combat the effects of noise. However, large capacitance affect the accuracy of the temperature measurement, leading to a recommended maximum capacitor value of 1000 pF. This capacitor reduces the noise, but does not eliminate it, which makes using the sensor difficult in a very noisy environment.

The ADT7490 has a major advantage over other devices for eliminating the effects of noise on the external sensor. Using the series resistance cancellation feature, a filter can be constructed between the external temperature sensor and the part. The effect of any filter resistance seen in series with the remote sensor is automatically canceled from the temperature result.

The construction of a filter allows the ADT7490 and the remote temperature sensor to operate in noisy environments. Figure 28 shows a low−pass RC filter with the following values:

$$R = 100\ \Omega, C = 1\ nF \quad \text{(eq. 3)}$$

This filtering reduces both common−mode noise and differential noise.

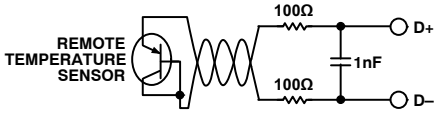


Figure 28. Filter Between Remote Sensor and ADT7490

Factors Affecting Diode Accuracy

Remote Sensing Diode

The ADT7490 is designed to work with either substrate transistors built into processors or discrete transistors. Substrate transistors are generally PNP types with the collector connected to the substrate. Discrete types can be either PNP or NPN transistors connected as a diode (base−shorted to the collector). To reduce the error due to variations in both substrate and discrete transistors, a number of factors should be taken into consideration:

- The ideality factor, n_f, of the transistor is a measure of the deviation of the thermal diode from ideal behavior. The ADT7490 is trimmed for an n_f value of 1.008. Use the following equation to calculate the error introduced at a temperature T (°C) when using a transistor whose n_f does not equal 1.008. Refer to the data sheet for the related CPU to obtain the n_f values.

$$\Delta T = (nf - 1.008)/1.008 \times (273.15\ K + T) \quad \text{(eq. 4)}$$

To factor this in, the user can write the ΔT value to the offset register. The ADT7490 automatically adds it to or subtracts it from the temperature measurement.

- Some CPU manufacturers specify the high and low current levels of the substrate transistors. The high current level of the ADT7490, I_{HIGH}, is 192 μA and the low level current, I_{LOW}, is 12 μA. If the ADT7490 current levels do not match the current levels specified by the CPU manufacturer, it may be necessary to remove an offset. The CPU's data sheet advises whether this offset needs to be removed and how to calculate it. This offset can be programmed to the offset register. It is important to note that if more than one offset must be considered, the algebraic sum of these offsets must be programmed to the offset register.

If a discrete transistor is used with the ADT7490, the best accuracy is obtained by choosing devices according to the following criteria:

- Base−emitter voltage greater than 0.25 V at 12 μA at the highest operating temperature.
- Base−emitter voltage less than 0.95 V at 192 μA at the lowest operating temperature.
- Base resistance less than 100 Ω.
- Small variation in h_{FE} (such as 50 to 150) that indicates tight control of V_{BE} characteristics.

Transistors, such as 2N3904, 2N3906, or equivalents in SOT−23 packages, are suitable devices to use.

Reading Temperature from the ADT7490

It is important to note that temperature can be read from the ADT7490 as an 8−bit value (with 1°C resolution) or as a 10−bit value (with 0.25°C resolution). If only 1°C resolution is required, the temperature readings can be read back at any time and in no particular order.

If the 10−bit measurement is required, it involves a 2−register read for each measurement. The Extended Resolution 2 register (0x77) should be read first. This causes all temperature reading registers to be frozen until all temperature reading registers have been read from. This prevents an MSB reading from being updated while its two LSBs are being read and vice versa.

Nulling Out Temperature Errors

As CPUs run faster, it becomes more difficult to avoid high frequency clocks when routing the D+/D− traces around a system board. Even when recommended layout guidelines are followed, some temperature errors may still be attributable to noise coupled onto the D+/D− lines. Constant high frequency noise usually attenuates or increases temperature measurements by a linear, constant value.

The ADT7490 has temperature offset registers at Address 0x70, Address 0x71, and Address 0x72 for the Remote 1, local, and Remote 2 temperature channels, respectively. By performing a one−time calibration of the system, the user can determine the offset caused by system board noise and null it out using the offset registers. The offset registers automatically add a twos complement 8−bit reading to every temperature measurement.

The temperature offset range and resolution is selected by setting Bit 1 of Register 0x7C. This ensures that the readings in the temperature measurement registers are as accurate as possible. Setting this bit to 0 means the LSBs add 0.5°C offset to the temperature reading, so the 8−bit register effectively allows temperature offsets from −63°C to +64°C with a resolution of 0.5°C. Setting this bit to 1 means the LSBs add 1°C offset to the temperature reading, so the 8−bit register effectively allows temperature offsets of up to −63°C to +127°C with a resolution of 1°C. For the PECI offset registers, the resolution is always 1°C.

Temperature Offset Registers

Register 0x70, Remote 1 Temperature Offset = 0x00 (0°C default)

Register 0x71, Local Temperature Offset = 0x00 (0°C default)

Register 0x72, Remote 2 Temperature Offset = 0x00 (0°C default)

Register 0x94, PECI0 Temperature Offset = 0x00 (0°C default)

Register 0x95, PECI1 Temperature Offset = 0x00 (0°C default)

Register 0x96, PECI2 Temperature Offset = 0x00 (0°C default)

Register 0x97, PECI3 Temperature Offset = 0x00 (0°C default)

Temperature Measurement Limit Registers

Associated with each temperature measurement channel are high and low limit registers. Exceeding the programmed high or low limit causes the appropriate status bit to be set. Exceeding either limit can also generate $\overline{\text{SMBALERT}}$ interrupts (depending on the way the interrupt mask register is programmed and assuming that $\overline{\text{SMBALERT}}$ is set as an output on the appropriate pin).

Additional ADC Functions for Temperature Measurement

A number of other functions are available on the ADT7490 to offer the system designer increased flexibility.

Turn−Off Averaging

For each temperature measurement read from a value register, 16 readings have actually been made internally, and the results averaged, before being placed into the value register. Sometimes it is necessary to take a very fast measurement. Setting Bit 4 of Configuration Register 2 (0x73) turns averaging off. The default round−robin cycle time with averaging off is a maximum of 23 ms.

Table 13. Conversion Time with Averaging Disabled

Channel	Measurement Time (ms)
Voltage Channels	0.7
Remote Temperature 1	7
Remote Temperature 2	7
Local Temperature	1.3

When Bit 7 of Configuration Register 6 (0x10) is set, the default round−robin cycle time increases to a maximum of 193 ms.

Table 14. Conversion Time with Averaging Enabled

Channel	Measurement Time (ms)
Voltage Channels	11
Remote Temperature	39
Local Temperature	12

Single−Channel ADC Conversions

Setting Bit 6 of Configuration Register 2 (Register 0x73) places the ADT7490 into single−channel ADC conversion mode. In this mode, the ADT7490 can be made to read a single temperature channel only. The appropriate ADC channel is selected by writing to Bits [7:4] of the TACH1 Minimum High Byte register (0x55).

Table 15. Programming Single−Channel ADC Mode for Temperatures

Bits [7:4], Register 0x55	Channel Selected
Remote 1 Temperature	0101
Local Temperature	0110
Remote 2 Temperature	0111

Configuration Register 2 (Register 0x73)

Bit 4 (AVG) = 1, averaging off.

Bit 6 (CONV) = 1, single−channel convert mode.

Overtemperature Events

Overtemperature events on any of the temperature channels can be detected and dealt with automatically in automatic fan speed control mode. Register 0x6A to Register 0x6C are the $\overline{\text{THERM}}$ temperature limits for the local and remote diode temperature channels. The equivalent PECI limit is $T_{CONTROL}$ in Register 0x3D. When a temperature exceeds its $\overline{\text{THERM}}$ temperature limit, all PWM outputs run at 100% duty cycle (default). This can be changed to maximum PWM duty cycle as programmed in Register 0x38, Register 0x39, and Register 0x3A, by setting Bit 3 of Register 0x7D.

The fans run at this speed until the temperature drops below $\overline{\text{THERM}}$ minus hysteresis. This can be disabled by setting the BOOST bit in Configuration Register 3, Bit 2 (0x78). The hysteresis value for the $\overline{\text{THERM}}$ temperature limit is the value programmed into the hysteresis registers (0x6D and 0x6E). The default hysteresis value is 4°C.

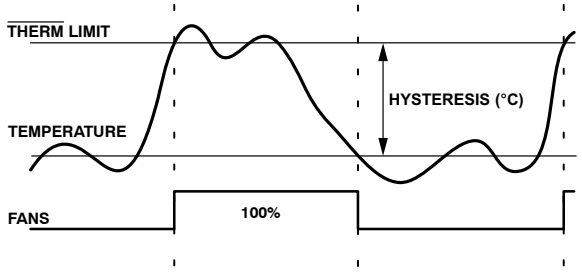


Figure 29. $\overline{\text{THERM}}$ Temperature Limit Operation

$\overline{\text{THERM}}$ can be disabled by setting Bit 2 of Configuration Register 4 (0x7D). $\overline{\text{THERM}}$ can also be disabled by:

- In Offset 64 mode, writing −64°C to the appropriate $\overline{\text{THERM}}$ temperature limit.
- In twos complement mode, writing −128°C to the appropriate $\overline{\text{THERM}}$ temperature limit.

Limits, Status Registers, and Interrupts

Limit Values

Associated with each measurement channel on the ADT7490 are high and low limits. These can form the basis of system status monitoring; a status bit can be set for any out−of−limit condition and is detected by polling the device. Alternatively, $\overline{\text{SMBALERT}}$ interrupts can be generated to flag out−of−limit conditions to a processor or micro−controller.

8−Bit Limits

The following is a list of 8−bit limits on the ADT7490:

Voltage Limit Registers

Register 0x44, +2.5 V_{IN} Low Limit = 0x00 default

Register 0x45, +2.5 V_{IN} High Limit = 0xFF default

Register 0x46, V_{CCP} Low Limit = 0x00 default

Register 0x47, V_{CCP} High Limit = 0xFF default

Register 0x48, V_{CC} Low Limit = 0x00 default

Register 0x49, V_{CC} High Limit = 0xFF default

Register 0x4A, +5 V_{IN} Low Limit = 0x00 default

Register 0x4B, +5 V_{IN} High Limit = 0xFF default

Register 0x4C, +12 V_{IN} Low Limit = 0x00 default

Register 0x4D, +12 V_{IN} High Limit = 0xFF default

Register 0x84, V_{TT} Low Limit = 0x00 default

Register 0x86, V_{TT} High Limit = 0xFF default

Register 0x85, I_{MON} Low Limit = 0x00 default

Register 0x87, I_{MON} High = 0xFF default

Temperature Limit Registers

Register 0x4E, Remote 1 Temperature Low Limit = 0x81 default

Register 0x4F, Remote 1 Temperature High Limit = 0x7F default

Register 0x6A, Remote 1 $\overline{\text{THERM}}$ Temperature Limit = 0x64 default

Register 0x50, Local Temperature Low Limit = 0x81 default

Register 0x51, Local Temperature High Limit = 0x7F default

Register 0x6B, Local $\overline{\text{THERM}}$ Temperature Limit = 0x64 default
Register 0x52, Remote 2 Temperature Low Limit = 0x81 default
Register 0x53, Remote 2 Temperature High Limit = 0x7F default
Register 0x6C, Remote 2 $\overline{\text{THERM}}$ Temperature Limit = 0x64 default
Register 0x34, PECI Low Limit = 0x81 default
Register 0x35, PECI High Limit = 0x00 default
Register 0x3D, PECI $T_{CONTROL}$ Limit = 0x00 default

$\overline{\text{THERM}}$ Timer Limit Register

Register 0x7A, $\overline{\text{THERM}}$ Timer Limit = 0x00 default

16−Bit Limits

The fan TACH measurements are 16−bit results. The fan TACH limits are also 16 bits, consisting of a high byte and low byte. Only high limits exist for fan TACHs because fans running under speed or stalled are normally the only conditions of interest. Because the fan TACH period is actually being measured, exceeding the limit indicates a slow or stalled fan.

Fan Limit Registers

Register 0x54, TACH1 Minimum Low Byte = 0xFF default
Register 0x55, TACH1 Minimum High Byte = 0xFF default
Register 0x56, TACH2 Minimum Low Byte = 0xFF default
Register 0x57, TACH2 Minimum High Byte = 0xFF default
Register 0x58, TACH3 Minimum Low Byte = 0xFF default
Register 0x59, TACH3 Minimum High Byte = 0xFF default
Register 0x5A, TACH4 Minimum Low Byte = 0xFF default
Register 0x5B, TACH4 Minimum High Byte = 0xFF default

Out−of−Limit Comparisons

Once all limits have been programmed, the ADT7490 can be enabled for monitoring. The ADT7490 measures all voltage and temperature measurements in round−robin format and sets the appropriate status bit to indicate out−of−limit conditions. TACH measurements are not part of this round−robin cycle. Comparisons are done differently depending on whether the measured value is being compared to a high or low limit.

High Limit > Comparison Performed
Low Limit ≤ Comparison Performed

Voltage and temperature channels use a window comparator for error detecting and, therefore, have high and low limits. Fan speed measurements use only a low limit.

Analog Monitoring Cycle Time

The analog monitoring cycle begins when a 1 is written to the start bit (Bit 0) of Configuration Register 1 (0x40). The ADC measures each analog input in turn and, as each measurement is completed, the result is automatically stored in the appropriate value register. This round−robin monitoring cycle continues unless disabled by writing a 0 to Bit 0 of Configuration Register 1.

As the ADC is normally left to free−run in this manner, the time taken to monitor all the analog inputs is normally not of interest, because the most recently measured value of any input can be read out at any time. For applications where the monitoring cycle time is important, it can easily be calculated.

The total number of channels measured consists of

- Six dedicated supply voltage inputs
- Supply voltage (V_{CC} pin)
- Local temperature
- Two remote temperatures

As mentioned previously, the ADC performs round−robin conversions and takes 11 ms for each voltage measurement, 12 ms for a local temperature reading, and 39 ms for each remote temperature reading. The total monitoring cycle time for averaged voltage and temperature monitoring is, therefore, nominally

$$(7 \times 11) + 12 + (2 \times 39) = 167 \text{ ms} \quad \text{(eq. 5)}$$

Fan TACH measurements and PECI thermal measurements are made in parallel and are not synchronized with the analog measurements in any way.

Interrupt Status Registers

The results of limit comparisons are stored in Interrupt Status Register 1 to Interrupt Status Register 4. The status register bit for each channel reflects the status of the last measurement and limit comparison on that channel. If a measurement is within limits, the corresponding interrupt status register bit is cleared to 0. If the measurement is out of limit, the corresponding interrupt status register bit is set to 1.

The state of the various measurement channels can be polled by reading the interrupt status registers over the serial bus. In Bit 7 (OOL) of Interrupt Status Register 1 (0x41), a Logic 1 indicates an out−of−limit event has been flagged in Interrupt Status Register 2. This means the user also needs to read Interrupt Status Register 2. There is a similar OOL bit in Interrupt Status Register 2 and Interrupt Status Register 3, indicating an out−of−limit event in the next status register.

Alternatively, Pin 10 or Pin 14 can be configured as an $\overline{\text{SMBALERT}}$ output. This hard interrupt automatically notifies the system supervisor of an out−of−limit condition. Reading the interrupt status registers clears the appropriate status bit as long as the error condition that caused the interrupt has cleared. Interrupt status register bits are sticky. Whenever an interrupt status bit is set, indicating an out−of−limit condition, it remains set even if the event that caused it has gone away (until read).

The only way to clear the interrupt status bit is to read the interrupt status register after the event has gone away. Interrupt status mask registers allow individual interrupt sources to be masked from causing an $\overline{\text{SMBALERT}}$ on the dedicated alert pin. However, if one of these masked interrupt sources goes out of limit, its associated interrupt status bit is set in the interrupt status registers.

Full details of the Interrupt Status and Interrupt Mask registers associated with each measurement channels are detailed in the Table 16 and in the full register map in the Register Tables section.

Table 16. Interrupt Status and Interrupt Mask Register Address and Bit Assignments

Interrupt Status Register	Interrupt Mask Register	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x41	0x74	OOL	R2T	LT	R1T	+5 V_{IN}	V_{CC}	V_{CCP}	+2.5 V_{IN}/$\overline{THERM}$
0x42	0x75	D2 FAULT	D1 FAULT	FAN4/$\overline{THERM}$	FAN3	FAN2	FAN1	OOL	+12 V_{IN}
0x43	0x82	OOL	RES	RES	RES	OVT	COM M	DATA	PECI0
0x81	0x83	V_{TT}	I_{MON}	PECI3	PECI2	PECI1	RES	RES	RES

$\overline{SMBALERT}$ Interrupt Behavior

The ADT7490 can be polled for status, or an $\overline{SMBALERT}$ interrupt can be generated for out−of−limit conditions. It is important to note how the $\overline{SMBALERT}$ output and status bits behave when writing interrupt handler software.

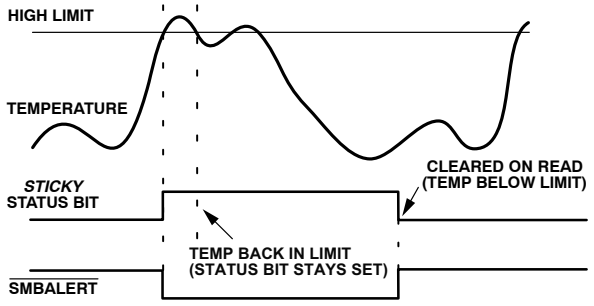


Figure 30. $\overline{SMBALERT}$ and Status Bit Behavior

Figure 30 shows how the $\overline{SMBALERT}$ output and sticky status bits behave. Once a limit is exceeded, the corresponding status bit is set to 1. The status bit remains set until the error condition subsides and the status register is read. The status bits are referred to as sticky, because they remain set until read by software. This ensures that an out−of−limit event cannot be missed if software is polling the device periodically.

Note that the $\overline{SMBALERT}$ output remains low for the entire duration that a reading is out of limit and until the status register has been read. This has implications on how software handles the interrupt.

Handling $\overline{SMBALERT}$ Interrupts

To prevent the system from being tied up servicing interrupts, it is recommend to handle the $\overline{SMBALERT}$ interrupt as follows:

1. Detect the $\overline{SMBALERT}$ assertion.
2. Enter the interrupt handler.
3. Read the status registers to identify the interrupt source.
4. Mask the interrupt source by setting the appropriate mask bit in the interrupt mask registers (0x74, 0x75, 0x82, and 0x83).
5. Take the appropriate action for a given interrupt source.
6. Exit the interrupt handler.
7. Periodically poll the status registers. If the interrupt status bit has cleared, reset the corresponding interrupt mask bit to 0. This causes the $\overline{SMBALERT}$ output and status bits to behave as shown in Figure 31.

Masking Interrupt Sources

The interrupt mask registers allow individual interrupt sources to be masked out to prevent $\overline{SMBALERT}$ interrupts. Note that masking an interrupt source prevents only the $\overline{SMBALERT}$ output from being asserted; the appropriate status bit is set normally (see Figure 31). Full details of the status and mask registers associated with each measurement channel are detailed in Table 16 and Table 20.

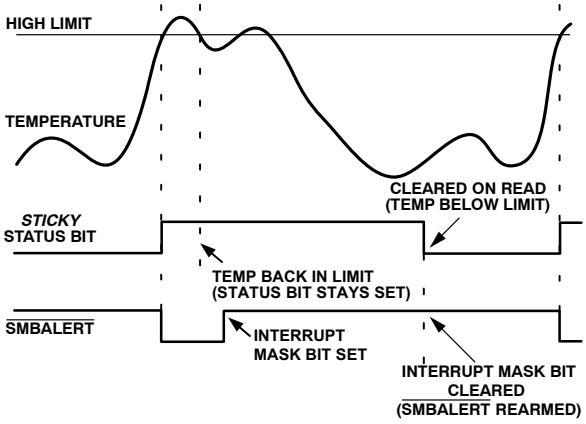


Figure 31. How Masking the Interrupt Source Affects $\overline{SMBALERT}$ Output

Enabling the $\overline{SMBALERT}$ Interrupt Output

The $\overline{SMBALERT}$ interrupt function is disabled by default. Pin 10 or Pin 14 can be reconfigured as an $\overline{SMBALERT}$ output to signal out−of−limit conditions.

Table 17. Configuring Pin 10 as $\overline{SMBALERT}$ Output

Register	Bit Setting
Configuration Register 3 (Register 0x78), Bit 0	[1] Pin 10 = $\overline{SMBALERT}$ [0] Pin 10 = PWM2 (default)

Assigning $\overline{THERM}$ Functionality to a Pin

Pin 14 on the ADT7490 has three possible functions: $\overline{SMBALERT}$, $\overline{THERM}$, and TACH4. The user chooses the required functionality by setting Bit 0 and Bit 1 of Configuration Register 4 at Address 0x7D.

If $\overline{\text{THERM}}$ is enabled (Bit 1, Configuration Register 3 at Address 0x78),

- Pin 22 becomes $\overline{\text{THERM}}$.
- If Pin 14 is configured as $\overline{\text{THERM}}$ (Bit 0 and Bit 1 of Configuration Register 4 at Address 0x7D), $\overline{\text{THERM}}$ is enabled on this pin.

If $\overline{\text{THERM}}$ is not enabled,

- Pin 22 becomes a 2.5 V_{IN} measurement input.
- If Pin 14 is configured as $\overline{\text{THERM}}$, $\overline{\text{THERM}}$ is disabled on this pin.

Table 18. Configuring Pin 14 in Register 0x7D

Bit 1	Bit 0	Function
0	0	TACH4
0	1	$\overline{\text{THERM}}$
1	0	$\overline{\text{SMBALERT}}$
1	1	Reserved

$\overline{\text{THERM}}$ as an Input

When $\overline{\text{THERM}}$ is configured as an input, the user can time assertions on the $\overline{\text{THERM}}$ pin. This can be useful for connecting to the $\overline{\text{PROCHOT}}$ output of a CPU to gauge system performance.

The user can also set up the ADT7490 so that the fans run at 100% when the $\overline{\text{THERM}}$ pin is driven low externally. The fans run at 100% for the duration of the time that the $\overline{\text{THERM}}$ pin is pulled low. This is done by setting the BOOST bit (Bit 2) in Configuration Register 3 (Address 0x78) to 1. This works only if the fan is already running, for example, in manual mode when the current duty cycle is above 0x00, or in automatic mode when the temperature is above T_{MIN}.

If the temperature is below T_{MIN} or if the duty cycle in manual mode is set to 0x00, pulling the $\overline{\text{THERM}}$ low externally has no effect. See Figure 32 for more information.

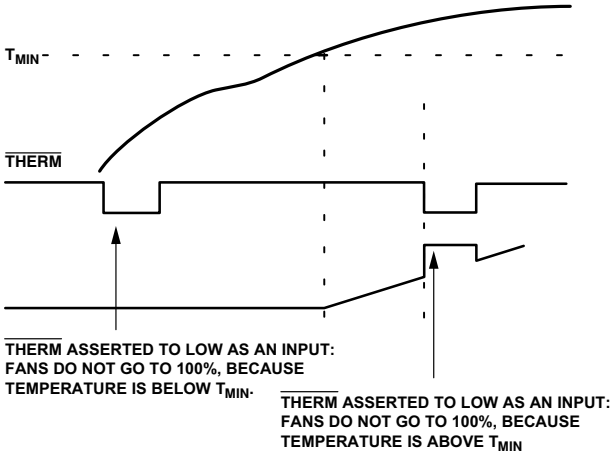


Figure 32. Asserting $\overline{\text{THERM}}$ Low as an Input in Automatic Fan Speed Control Mode

$\overline{\text{THERM}}$ Timer

The ADT7490 has an internal timer to measure $\overline{\text{THERM}}$ assertion time. For example, the $\overline{\text{THERM}}$ input can be connected to the $\overline{\text{PROCHOT}}$ output of a CPU to measure system performance. The $\overline{\text{THERM}}$ input can also be connected to the output of a trip point temperature sensor.

The timer is started on the assertion of the ADT7490 $\overline{\text{THERM}}$ input and stopped when $\overline{\text{THERM}}$ is deasserted. The timer counts $\overline{\text{THERM}}$ times cumulatively, that is, the timer resumes counting on the next $\overline{\text{THERM}}$ assertion. The $\overline{\text{THERM}}$ timer continues to accumulate $\overline{\text{THERM}}$ assertion times until the timer is read (it is cleared on read), or until it reaches full scale. If the counter reaches full scale, it stops at that reading until cleared.

The 8−bit $\overline{\text{THERM}}$ timer status register (0x79) is designed so that Bit 0 is set to 1 on the first $\overline{\text{THERM}}$ assertion. Once the cumulative $\overline{\text{THERM}}$ assertion time has exceeded 45.52 ms, Bit 1 of the $\overline{\text{THERM}}$ timer is set and Bit 0 now becomes the LSB of the timer with a resolution of 22.76 ms (see Figure 33).

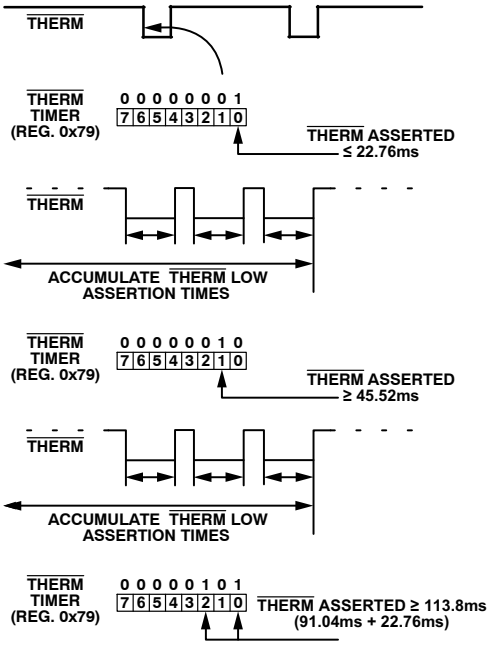


Figure 33. Understanding the $\overline{\text{THERM}}$ Timer

When using the $\overline{\text{THERM}}$ timer, be aware of the following:

After a $\overline{\text{THERM}}$ timer read (Register 0x79):

- The contents of the timer are cleared on read.
- Bit 5 of Interrupt Status 2 register (0x42) needs to be cleared (assuming that the $\overline{\text{THERM}}$ timer limit has been exceeded).

If the $\overline{\text{THERM}}$ timer is read during a $\overline{\text{THERM}}$ assertion, the following happens:

- The contents of the timer are cleared.
- Bit 0 of the $\overline{\text{THERM}}$ timer is set to 1, because a $\overline{\text{THERM}}$ assertion is occurring.
- The $\overline{\text{THERM}}$ timer increments from zero.
- If the $\overline{\text{THERM}}$ timer limit (Register 0x7A) = 0x00, the F4P bit is set.

Generating $\overline{\text{SMBALERT}}$ Interrupts from $\overline{\text{THERM}}$ Timer Events

The ADT7490 can generate $\overline{\text{SMBALERT}}$s when a programmable $\overline{\text{THERM}}$ timer limit has been exceeded. This allows the system designer to ignore brief, infrequent $\overline{\text{THERM}}$ assertions while capturing longer $\overline{\text{THERM}}$ timer events. Register 0x7A is the $\overline{\text{THERM}}$ timer limit register. This 8−bit register allows a limit from 0 sec (first $\overline{\text{THERM}}$ assertion) to 5.825 sec to be set before an $\overline{\text{SMBALERT}}$ is generated. The $\overline{\text{THERM}}$ timer value is compared with the contents of the $\overline{\text{THERM}}$ timer limit register. If the $\overline{\text{THERM}}$ timer value exceeds the $\overline{\text{THERM}}$ timer limit value, the FAN4 bit (Bit 5) of Status Register 2 is set and an $\overline{\text{SMBALERT}}$ is generated.

Note that depending on which pins are configured as a $\overline{\text{THERM}}$ timer, setting the FAN4/$\overline{\text{THERM}}$ bit (Bit 5) of the Interrupt Mask Register 2 (0x75), or bit 0 of the Interrupt Mask Register 1 (0x74), masks out $\overline{\text{SMBALERT}}$; although the FAN4 bit of Interrupt Status Register 2 is still set if the $\overline{\text{THERM}}$ timer limit is exceeded.

Figure 34 is a functional block diagram of the $\overline{\text{THERM}}$ timer, $\overline{\text{THERM}}$ limit, and its associated circuitry. Writing a value of 0x00 to the $\overline{\text{THERM}}$ Timer Limit register (0x7A) causes an $\overline{\text{SMBALERT}}$ to be generated on the first $\overline{\text{THERM}}$ assertion. A $\overline{\text{THERM}}$ timer limit value of 0x01 generates an $\overline{\text{SMBALERT}}$ once cumulative $\overline{\text{THERM}}$ assertions exceed 45.52 ms.

Configuring the Relevant $\overline{\text{THERM}}$ Behavior

1. Configure the desired pin as the $\overline{\text{THERM}}$ timer input. Setting Bit 1 ($\overline{\text{THERM}}$ timer enable) of Configuration Register 3 (Register 0x78) enables the $\overline{\text{THERM}}$ timer monitoring functionality. This is disabled on Pin 14 and Pin 22 by default.
   Setting Bit 0 and Bit 1 (Pin 14 Func) of Configuration Register 4 (Register 0x7D) enables $\overline{\text{THERM}}$ timer output functionality on Pin 22 (Bit 1 of Configuration Register 3, $\overline{\text{THERM}}$, must also be set). Pin 14 can also be used as TACH4.
2. Select the desired fan behavior for $\overline{\text{THERM}}$ timer events. Assuming the fans are running, setting Bit 2 (BOOST bit) of Configuration Register 3 (Register 0x78) causes all fans to run at 100% duty cycle whenever $\overline{\text{THERM}}$ is asserted.
   This allows fail−safe system cooling. If this bit = 0, the fans run at their current settings and are not affected by $\overline{\text{THERM}}$ events. If the fans are not already running when $\overline{\text{THERM}}$ is asserted, the fans do not run to full speed.
3. Select whether $\overline{\text{THERM}}$ timer events should generate $\overline{\text{SMBALERT}}$ interrupts.
   Bit 5 of Interrupt Mask Register 2 (0x75) or Bit 0 of Interrupt Mask Register 1 (0x74), depending on which pins are configured as a THERM timer, when set, masks out $\overline{\text{SMBALERT}}$s when the $\overline{\text{THERM}}$ timer limit value is exceeded. This bit should be cleared if $\overline{\text{SMBALERT}}$s based on $\overline{\text{THERM}}$ events are required.
4. Select a suitable $\overline{\text{THERM}}$ limit value.
   This value determines whether an $\overline{\text{SMBALERT}}$ is generated on the first $\overline{\text{THERM}}$ assertion, or only if a cumulative $\overline{\text{THERM}}$ assertion time limit is exceeded. A value of 0x00 causes an $\overline{\text{SMBALERT}}$ to be generated on the first $\overline{\text{THERM}}$ assertion.
5. Select a $\overline{\text{THERM}}$ monitoring time.
   This value specifies how often OS− or BIOS−level software checks the $\overline{\text{THERM}}$ timer. For example, BIOS can read the $\overline{\text{THERM}}$ timer once an hour to determine the cumulative $\overline{\text{THERM}}$ assertion time. If, for example, the total $\overline{\text{THERM}}$ assertion time is <22.76 ms in Hour 1, >182.08 ms in Hour 2, and >2.914 sec in Hour 3, this indicates that system performance is degrading significantly because $\overline{\text{THERM}}$ is asserting more frequently on an hourly basis.

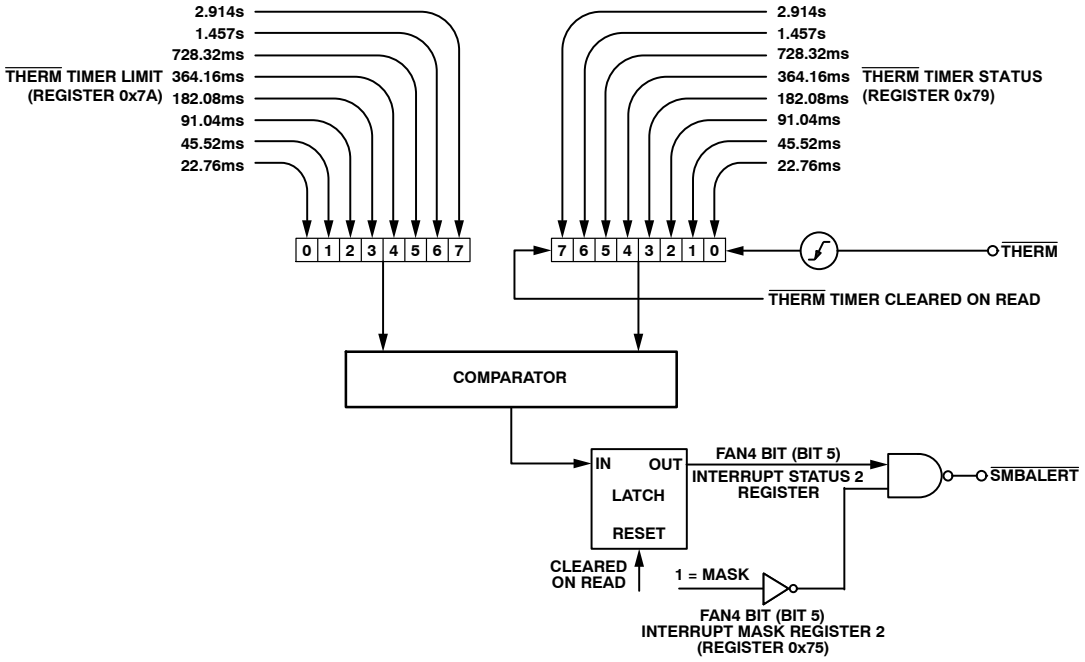


Figure 34. Functional Block Diagram of THERM Monitoring Circuitry

Alternatively, OS− or BIOS−level software can time−stamp when the system is powered on. If an SMBALERT is generated due to the THERM timer limit being exceeded, another time−stamp can be taken. The difference in time can be calculated for a fixed THERM timer limit time. For example, if it takes one week for a THERM timer limit of 2.914 sec to be exceeded, and the next time it takes only 1 hour, this is an indication of a serious degradation in system performance.

Configuring the THERM Pin as an Output

In addition to monitoring THERM as an input, the ADT7490 can optionally drive THERM low as an output. When PROCHOT is bidirectional, THERM can be used to throttle the processor by asserting PROCHOT. The user can preprogram system−critical thermal limits. If the temperature exceeds a thermal limit by 0.25°C, THERM asserts low. If the temperature is still above the thermal limit on the next monitoring cycle, THERM stays low. THERM remains asserted low until the temperature is equal to or below the thermal limit. Because the temperature for that channel is measured only once for every monitoring cycle, after THERM asserts, it is guaranteed to remain low for at least one monitoring cycle.

The THERM pin can be configured to assert low if the Remote 1 THERM, local THERM, Remote 2 THERM or PECI temperature limits are exceeded by 0.25°C. The THERM temperature limit registers are at Register 0x6A, Register 0x6B, and Register 0x6C, respectively. Setting Bits [5:7] of Configuration Register 5 (0x7C) enables the THERM output feature for the Remote 1, local, and Remote 2 temperature channels, respectively. Figure 35 shows how the THERM pin asserts low as an output in the event of a critical overtemperature.

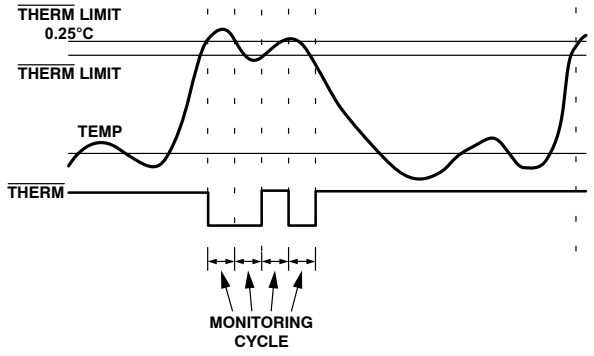


Figure 35. Asserting THERM as an Output, Based on Tripping THERM Limits

An alternative method of disabling THERM is to program the THERM temperature limit to –63°C or less in Offset 64 mode, or −128°C or less in twos complement mode; that is, for THERM temperature limit values less than –63°C or –128°C, respectively, THERM is disabled.

Enabling and Disabling THERM on Individual Channels.

The THERM pin can be enabled/disabled for individual or combinations of temperature channels using Bits [7:5] of Configuration Register 5 (0x7C).

$\overline{\text{THERM}}$ Hysteresis

Setting Bit 0 of Configuration Register 7 (0x11) disables $\overline{\text{THERM}}$ hysteresis.

If $\overline{\text{THERM}}$ hysteresis is enabled and $\overline{\text{THERM}}$ is disabled (Bit 2 of Configuration Register 4, 0x7D), the $\overline{\text{THERM}}$ event is not reflected in the status register and the fans do not go to full speed. If $\overline{\text{THERM}}$ hysteresis is disabled and $\overline{\text{THERM}}$ is disabled (Bit 2 of Configuration Register 4, 0x7D) and assuming the appropriate pin is configured as $\overline{\text{THERM}}$, the $\overline{\text{THERM}}$ pin asserts low when a $\overline{\text{THERM}}$ event occurs.

If $\overline{\text{THERM}}$ and $\overline{\text{THERM}}$ hysteresis are both enabled, the $\overline{\text{THERM}}$ output asserts as expected.

$\overline{\text{THERM}}$ Operation in Manual Mode

In manual mode, $\overline{\text{THERM}}$ events do not cause fans to go to full speed, unless Bit 5 of Configuration Register 1 (0x40) is set to 1.

Additionally, Bit 3 of Configuration Register 4 (0x7D) can be used to select PWM speed on $\overline{\text{THERM}}$ event (100% or maximum PWM).

Bit 2 in Configuration Register 4 (0x7D) can be set to disable $\overline{\text{THERM}}$ events from affecting the fans.

Fan Drive Using PWM Control

The ADT7490 uses pulse−width modulation (PWM) to control fan speed. This relies on varying the duty cycle (or on/off ratio) of a square wave applied to the fan to vary the fan speed. The external circuitry required to drive a fan using PWM control is extremely simple. For 4−wire fans, the PWM drive may need only a pullup resistor. In many cases, the 4−wire fan PWM input has a built−in, pullup resistor.

The ADT7490 PWM frequency can be set to a selection of low frequencies or a single high PWM frequency. The low frequency options are used for 3−wire fans, while the high frequency option is usually used with 4−wire fans.

For 3−wire fans, a single N−channel MOSFET is the only drive device required. The specifications of the MOSFET depend on the maximum current required by the fan being driven and the input capacitance of the FET. Because a 10 kΩ (or greater) resistor must be used as a PWM pullup, an FET with large input capacitance can cause the PWM output to become distorted and adversely affect the fan control range. This is a requirement only when using high frequency PWM mode.

Typical notebook fans draw a nominal 170 mA, therefore, SOT devices can be used where board space is a concern. In desktops, fans typically draw 250 mA to 300 mA each. If several fans are driven in parallel from a single PWM output or drive larger server fans, the MOSFET must handle the higher current requirements. The only other stipulation is that the MOSFET should have a gate voltage drive, V_{GS} < 3.3 V, for direct interfacing to the PWM output pin. The MOSFET should also have a low on resistance to ensure that there is not a significant voltage drop across the FET, which would reduce the voltage applied across the fan and, therefore, the maximum operating speed of the fan.

Figure 36 shows how to drive a 3−wire fan using PWM control.

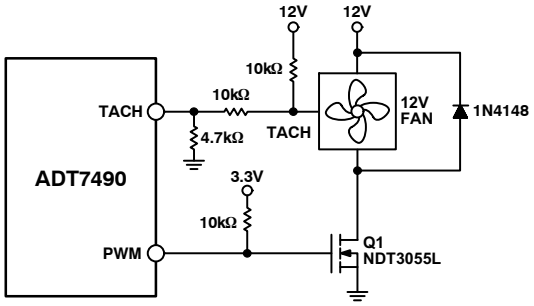


Figure 36. Driving a 3−Wire Fan Using an N−Channel MOSFET

Figure 36 uses a 10 kΩ pullup resistor for the TACH signal. This assumes that the TACH signal is an open−collector from the fan. In all cases, the TACH signal from the fan must be kept below 3.6 V maximum to prevent damaging the ADT7490.

Figure 37 shows a fan drive circuit using an NPN transistor such as a general−purpose MMBT2222. While these devices are inexpensive, they tend to have much lower current handling capabilities and higher on resistance than MOSFETs. When choosing a transistor, care should be taken to ensure that it meets the fan's current requirements. Ensure that the base resistor is chosen so that the transistor is saturated when the fan is powered on.

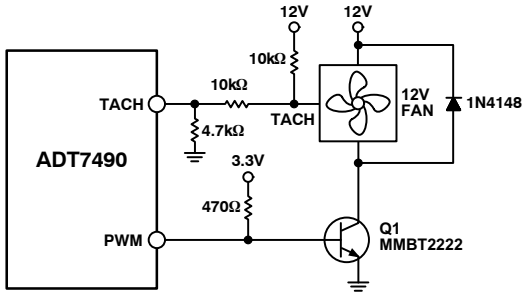


Figure 37. Driving a 3−Wire Fan Using an NPN Transistor

Because the fan drive circuitry in 4−wire fans is not switched on or off, as with previous PWM driven/powered fans, the internal drive circuit is always on and uses the PWM input as a signal instead of a power supply. This enables the internal fan drive circuit to perform better than 3−wire fans, especially for high frequency applications. Figure 38 shows a typical drive circuit for 4−wire fans.

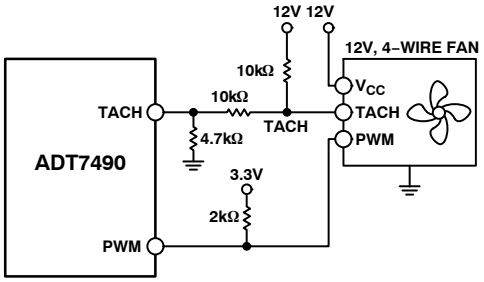


Figure 38. Driving a 4−Wire Fan

Driving Two Fans from PWM3

The ADT7490 has four TACH inputs available for fan speed measurement, but only three PWM drive outputs. If a fourth fan is being used in the system, it should be driven from the PWM3 output in parallel with the third fan.

Figure 39 shows how to drive two fans in parallel using low cost NPN transistors. Figure 40 shows the equivalent circuit using a MOSFET.

Because the MOSFET can handle up to 3.5 A, it is simply a matter of connecting another fan directly in parallel with the first. Care should be taken in designing drive circuits with transistors and FETs to ensure the PWM outputs are not required to source current, and that they sink less than the 5 mA maximum current specified in the data sheet.

Driving up to Three Fans from PWM3

TACH measurements for fans are synchronized to particular PWM channels; for example, TACH1 is synchronized to PWM1. TACH3 and TACH4 are both synchronized to PWM3, so PWM3 can drive two fans. Alternatively, PWM3 can be programmed to synchronize TACH2, TACH3, and TACH4 to the PWM3 output. This allows PWM3 to drive two or three fans. In this case, the drive circuitry looks the same, as shown in Figure 39 and Figure 40. The SYNC bit in Register 0x62 enables this function.

Synchronization is not required in high frequency mode when used with 4−wire fans.

SYNC, Enhanced Acoustics Register 1 (Register 0x62)

Bit 4 (SYNC) = 1, synchronizes TACH2, TACH3, and TACH4 to PWM3.

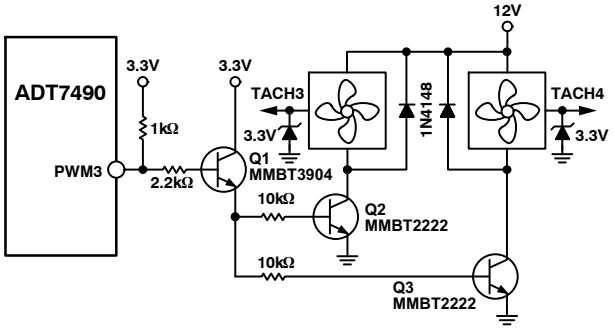


Figure 39. Interfacing Two Fans in Parallel to the PWM3 Output Using Low Cost NPN Transistors

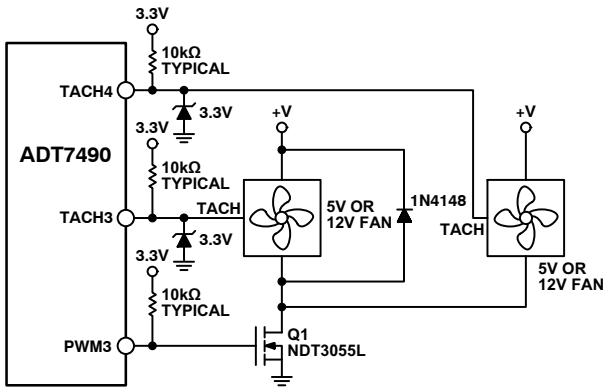


Figure 40. Interfacing Two Fans in Parallel to the PWM3 Output Using a Single N−Channel MOSFET

Laying Out 3−Wire Fans

Figure 41 shows how to lay out a common circuit arrangement for 3−wire fans.

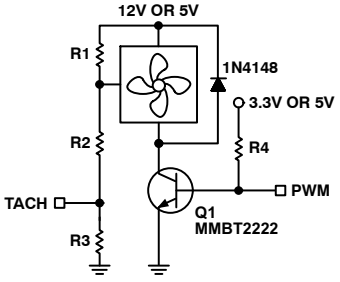


Figure 41. Planning for 3−Wire Fans on a PCB

TACH Inputs

Pin 9, Pin 11, Pin 12, and Pin 14 (when configured as TACH inputs) are high impedance inputs intended for fan speed measurement.

Signal conditioning in the ADT7490 accommodates the slow rise and fall times typical of fan tachometer outputs. The maximum input signal range is 0 V to 3.6 V, even though V_{CC} is 3.3 V. In the event that these inputs are supplied from fan outputs that exceed 0 V to 3.6 V, either resistive attenuation of the fan signal or diode clamping must be included to keep inputs within an acceptable range.

Figure 42 to Figure 45 show circuits for the most common fan TACH outputs.

If the fan TACH output has a resistive pullup to V_{CC}, it can be connected directly to the fan input, as shown in Figure 42.

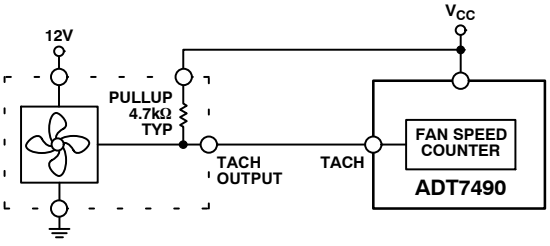


Figure 42. Fan with TACH Pullup to V_{CC}

If the fan output has a resistive pullup to 12 V, or other voltage greater than 3.6 V, the fan output can be clamped with a Zener diode, as shown in Figure 43. The Zener diode voltage should be chosen so that it is greater than V_{IH} of the TACH input but less than 3.6 V, allowing for the voltage tolerance of the Zener. A value of between 3.0 V and 3.6 V is suitable.

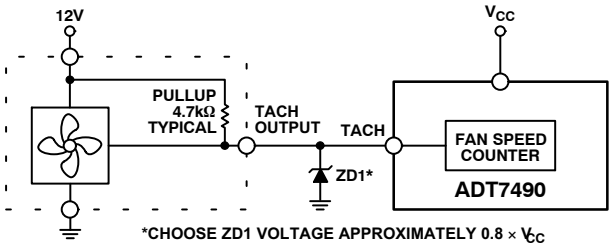


Figure 43. Fan with TACH Pullup to Voltage > 3.6 V, for Example, 12 V Clamped with Zener Diode

If the fan has a strong pullup (less than 1 kΩ) to 12 V or a totem−pole output, a series resistor can be added to limit the Zener current, as shown in Figure 44.

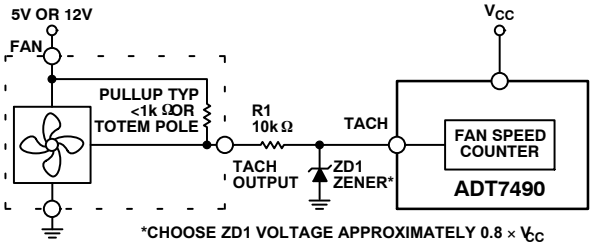


Figure 44. Fan with Strong TACH Pullup to >V_{CC} or Totem−Pole Output, Clamped with Zener Diode and Resistor

Alternatively, a resistive attenuator can be used, as shown in Figure 45. R1 and R2 should be chosen such that

$$2.0\ V < V_{PULLUP} \times R2/\left(R_{PULLUP} + R1 + R2\right) < 3.6\ V \quad \text{(eq. 6)}$$

The fan inputs have an input resistance of nominally 160 kΩ to ground, which should be taken into account when calculating resistor values.

With a pullup voltage of 12 V and pullup resistor less than 1 kΩ, suitable values for R1 and R2 are 100 kΩ and 40 kΩ, respectively. This gives a high input voltage of 3.42 V.

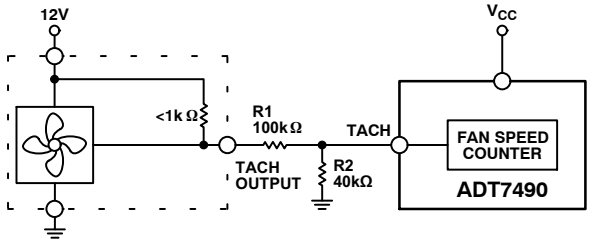


Figure 45. Fan with Strong TACH Pullup to >V_{CC} or Totem−Pole Output, Attenuated with R1/R2

The fan counter does not count the fan TACH output pulses directly because the fan speed could be less than 1000 RPM, and it takes several seconds to accumulate a reasonably large and accurate count. Instead, the period of the fan revolution is measured by gating an on−chip 90 kHz oscillator into the input of a 16−bit counter for N periods of the fan TACH output (see Figure 46), so the accumulated count is actually proportional to the fan tachometer period and inversely proportional to the fan speed.

N, the number of pulses counted, is determined by the settings of the TACH pulses per revolution register (0x7B). This register contains two bits for each fan, allowing one, two (default), three, or four TACH pulses to be counted.

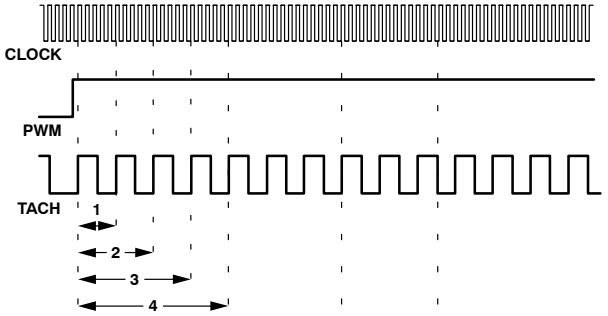


Figure 46. Fan Speed Measurement

Fan Speed Measurement Registers

The fan tachometer registers are 16−bit values consisting of a 2−byte read from the ADT7490.

Register 0x28, TACH1 Low Byte = 0x00 default
Register 0x29, TACH1 High Byte = 0x00 default
Register 0x2A, TACH2 Low Byte = 0x00 default
Register 0x2B, TACH2 High Byte = 0x00 default
Register 0x2C, TACH3 Low Byte = 0x00 default
Register 0x2D, TACH3 High Byte = 0x00 default
Register 0x2E, TACH4 Low Byte = 0x00 default
Register 0x2F, TACH4 High Byte = 0x00 default

Reading Fan Speed from the ADT7490

The measurement of fan speeds involves a 2−register read for each measurement. The low byte should be read first. This causes the high byte to be frozen until both high and low byte registers have been read, preventing erroneous TACH readings. The fan tachometer reading registers report back the number of 11.11 μs period clocks (90 kHz oscillator) gated to the fan speed counter, from the rising edge of the first fan TACH pulse to the rising edge of the third fan TACH pulse (assuming two pulses per revolution are being counted).

Because the device is essentially measuring the fan TACH period, the higher the count value, the slower the fan is actually running. A 16−bit fan tachometer reading of 0xFFFF indicates that either the fan has stalled or is running very slowly (<100 RPM).

High Limit > Comparison Performed

Because the actual fan TACH period is being measured, falling below a fan TACH limit by 1 sets the appropriate status bit and can be used to generate an $\overline{\text{SMBALERT}}$.

Fan TACH Limit Registers

The fan TACH limit registers are 16−bit values consisting of two bytes.

Register 0x54, TACH1 Minimum Low Byte = 0xFF default

Register 0x55, TACH1 Minimum High Byte = 0xFF default

Register 0x56, TACH2 Minimum Low Byte = 0xFF default

Register 0x57, TACH2 Minimum High Byte = 0xFF default

Register 0x58, TACH3 Minimum Low Byte = 0xFF default

Register 0x59, TACH3 Minimum High Byte = 0xFF default

Register 0x5A, TACH4 Minimum Low Byte = 0xFF default

Register 0x5B, TACH4 Minimum High Byte = 0xFF default

Fan Speed Measurement Rate

The fan TACH readings are normally updated once every second.

When set, the FAST bit (Bit 3) of Configuration Register 3 (0x78), updates the fan TACH readings every 250 ms.

DC Bits

If any of the fans are not being driven by a PWM channel but are powered directly from 5.0 V or 12 V, their associated dc bit in Configuration Register 3 should be set. This allows TACH readings to be taken on a continuous basis for fans connected directly to a dc source. For 4−wire fans, once high frequency mode is enabled, the dc bits do not need to be set because this is automatically done internally.

Calculating Fan Speed

Assuming a fan with a two pulses per revolution, and with the ADT7490 programmed to measure two pulses per revolution, fan speed is calculated by

Fan Speed (RPM) = (90,000 x 60)/Fan TACH Reading

where Fan TACH Reading is the 16−bit fan tachometer reading.

Example

TACH1 High Byte (Register 0x29) = 0x17

TACH1 Low Byte (Register 0x28) = 0xFF

What is Fan 1 speed in RPM?

Fan 1 TACH Reading = 0x17FF = 6143 (decimal)

RPM = (f x 60)/Fan 1 TACH Reading

RPM = (90000 x 60)/6143

Fan Speed = 879 RPM

Fan Pulses per Revolution

Different fan models can output either one, two, three, or four TACH pulses per revolution. Once the number of fan TACH pulses has been determined, it can be programmed into the TACH pulses per revolution register (0x7B) for each fan. Alternatively, this register can be used to determine the number or pulses per revolution output by a given fan. By plotting fan speed measurements at 100% speed with different pulses per revolution setting, the smoothest graph with the lowest ripple determines the correct pulses per revolution value.

TACH Pulses per Revolution Register

Bits [1:0], FAN1 default = 2 pulses per revolution

Bits [3:2], FAN2 default = 2 pulses per revolution

Bits [5:4], FAN3 default = 2 pulses per revolution

Bits [7:6], FAN4 default = 2 pulses per revolution

00 = 1 pulse per revolution
01 = 2 pulses per revolution
10 = 3 pulses per revolution
11 = 4 pulses per revolution

Fan Spin−Up

The ADT7490 has a unique fan spin−up function. It spins the fan at 100% PWM duty cycle until two TACH pulses are detected on the TACH input. When two TACH pulses have been detected, the PWM duty cycle goes to the expected running value, for example, 33%. The advantage of this is that fans have different spin−up characteristics and take different times to overcome inertia. The ADT7490 runs the fans just fast enough to overcome inertia and is quieter on spin−up than fans programmed to spin up for a given spin−up time.

Fan Startup Timeout

To prevent the generation of false interrupts as a fan spins up, because the fan is below running speed, the ADT7490 includes a fan startup timeout function. During this time, the ADT7490 looks for two TACH pulses. If two TACH pulses are not detected, an interrupt is generated.

Fan startup timeout can be disabled by setting Bit 3 (FSPDIS) of Configuration Register 7 (0x11).

PWM1, PWM2, PWM3 Configuration (Register 0x5C, Register 0x5D, Register 0x5E)

Bits [2:0] SPIN, startup timeout for PWM1 = 0x5C, PWM2 = 0x5D, and PWM3 = 0x5E.

000 = No startup timeout
001 = 100 ms
010 = 250 ms default
011 = 400 ms
100 = 667 ms
101 = 1 sec
110 = 2 sec
111 = 4 sec

Disabling Fan Startup Timeout

Although a fan startup makes fan spin−ups much quieter than fixed−time spin−ups, the option exists to use fixed spin−up times. Setting Bit 3 (FSPDIS) to 1 in Configuration Register 7 (Register 0x11) disables the spin−up for two TACH pulses. Instead, the fan spins up for the fixed time as selected in Register 0x5C to Register 0x5E.

PWM Logic State

The PWM outputs can be programmed high for 100% duty cycle (non−inverted) or low for 100% duty cycle (inverted).

PWM1 Configuration (Register 0x5C)

Bit 4 (INV)

0 = Logic high for 100% PWM duty cycle (non−inverted)
1 = Logic low for 100% PWM duty cycle (inverted)

PWM2 Configuration (Register 0x5D)

Bit 4 (INV)

0 = Logic high for 100% PWM duty cycle
1 = Logic low for 100% PWM duty cycle

PWM3 Configuration (Register 0x5E)

Bit 4 (INV)

0 = Logic high for 100% PWM duty cycle (non−inverted)
1 = Logic low for 100% PWM duty cycle (inverted).

Low Frequency Mode PWM Drive Frequency

The PWM drive frequency can be adjusted for the application. Register 0x5F to Register 0x61 configure the PWM frequency for PWM1 to PWM3, respectively.

PWM1, PWM 2, PWM3 Frequency Registers (Register 0x5F to Register 0x61)

Bits [2:0] FREQ

000 = 11.0 Hz
001 = 14.7 Hz
010 = 22.1 Hz
011 = 29.4 Hz
100 = 35.3 Hz default
101 = 44.1 Hz
110 = 58.8 Hz
111 = 88.2 Hz

High Frequency Mode PWM Drive

Setting Bit 3 of Register 0x5F, Register 0x60, and Register 0x61 enables high frequency mode for Fan 1, Fan 2, and Fan 3, respectively.

In high frequency mode, the PWM drive frequency is always 22.5 kHz. When high frequency mode is enabled, the dc bits are automatically asserted internally and do not need to be changed.

Fan Speed Control

The ADT7490 controls fan speed using automatic and manual modes.

In automatic fan speed control mode, fan speed is automatically varied with temperature and without CPU intervention, once initial parameters are set up. The advantage is that, if the system hangs, the user is guaranteed that the system is protected from overheating.

In manual fan speed control mode, the ADT7490 allows the duty cycle of any PWM output to be manually adjusted. This can be useful if the user wants to change fan speed in software or adjust PWM duty cycle output for test purposes. Bits [7:5] of Register 0x5C to Register 0x5E (PWM Configuration) control the behavior of each PWM output.

PWM Configuration Registers (Register 0x5C to Register 0x5E)

Bits [7:5] (BHVR)

111 = manual mode

Once under manual control, each PWM output can be manually updated by writing to Register 0x30 to Register 0x32 (PWMx current duty cycle registers).

Programming the PWM Current Duty Cycle Registers

The PWM current duty cycle registers are 8−bit registers that allow the PWM duty cycle for each output to be set anywhere from 0% to 100% in steps of 0.39%. The value to be programmed into the PWM_{MIN} register is given by

Value (decimal) = PWM_{MIN}/0.39%

Example 1

For a PWM duty cycle of 50%,
Value (decimal) = 50%/0.39% = 128 (decimal)
Value = 128 (decimal) or 0x80 (hexadecimal)

Example 2

For a PWM duty cycle of 33%,
Value (decimal) = 33%/0.39% = 85 (decimal)
Value = 85 (decimal) or 0x54 (hexadecimal)

PWM Duty Cycle Registers

Register 0x30, PWM1 Current Duty Cycle = 0xFF (100% default)
Register 0x31, PWM2 Current Duty Cycle = 0xFF (100% default)
Register 0x32, PWM3 Current Duty Cycle = 0xFF (100% default)

By reading the PWMx current duty cycle registers, the user can keep track of the current duty cycle on each PWM output, even when the fans are running in automatic fan speed control mode or acoustic enhancement mode.

Programming T_{RANGE}

T_{RANGE} defines the distance between T_{MIN} and 100% PWM. For the ADT7467, ADT7468, and ADT7473, T_{RANGE} is effectively a slope. For the ADT7475, ADT7476, and ADT7490, T_{RANGE} is no longer a slope but defines the temperature region where the PWM output linearly ramps from PWM_{MIN} to 100% PWM.

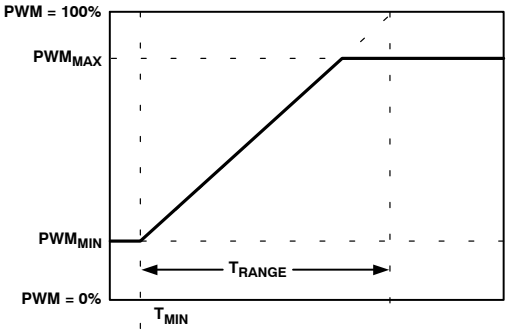


Figure 47. T_{RANGE}

Programming the Automatic Fan Speed Control Loop

To more efficiently understand the automatic fan speed control loop, using the ADT7490 evaluation board and software while reading this section is recommended.

This section provides the system designer with an understanding of the automatic fan control loop, and provides step−by−step guidance on effectively evaluating and selecting critical system parameters. To optimize the system characteristics, the designer needs to give some thought to system configuration, including the number of fans, where they are located, and what temperatures are being measured in the particular system.

The mechanical or thermal engineer who is tasked with the system thermal characterization should also be involved at the beginning of the system development process.

Manual Fan Control Overview

In unusual circumstances, it can be necessary to manually control the speed of the fans. Because the ADT7490 has an SMBus interface, a system can read back all necessary voltage, fan speed, and temperature information, and use this information to control the speed of the fans by writing to the current PWM duty cycle register (0x30, 0x31, and 0x32) of the appropriate fan. Bits [7:5] of the PWMx configuration registers (0x5C, 0x5D, and 0x5E) are used to set fans up for manual control.

$\overline{\text{THERM}}$ Operation in Manual Mode

In manual mode, if the temperature increases above the programmed $\overline{\text{THERM}}$ temperature limit, the fans automatically speed up to maximum PWM or 100% PWM, whichever way the appropriate fan channel is configured.

Automatic Fan Control Overview

The ADT7490 can automatically control the speed of fans based on the measured temperature. This is done independently of CPU intervention once the initial parameters are set up.

The ADT7490 has a local temperature sensor and two remote temperature channels that can be connected to a CPU on−chip thermal diode (available on Intel Pentium® class and other CPUs). These three temperature channels can be used as the basis for automatic fan speed control to drive fans using pulse−width modulation (PWM).

Automatic fan speed control reduces acoustic noise by optimizing fan speed according to accurately measured temperature. Reducing fan speed can also decrease system current consumption. The automatic fan speed control mode is very flexible due to the number of programmable parameters, including T_{MIN} and T_{RANGE}. The T_{MIN} and T_{RANGE} values for a temperature channel and, therefore, for a given fan are critical, because they define the thermal characteristics of the system. The thermal validation of the system is one of the most important steps in the design process, so these values should be selected carefully.

Figure 48 gives a top−level overview of the automatic fan control circuitry on the ADT7490. From a systems−level perspective, up to three system temperatures can be monitored and used to control three PWM outputs. The three PWM outputs can be used to control up to four fans. The ADT7490 allows the speed of four fans to be monitored. Each temperature channel has a thermal calibration block, allowing the designer to individually configure the thermal characteristics of each temperature channel. For example, users can decide to run the CPU fan when CPU temperature increases above 60°C and a chassis fan when the local temperature increases above 45°C.

At this stage, the designer has not assigned these thermal calibration settings to a particular fan drive (PWM) channel. The right side of Figure 48 shows controls that are fan−specific. The designer has individual control over parameters such as minimum PWM duty cycle, fan speed failure thresholds, and even ramp control of the PWM outputs. Automatic fan control ultimately allows graceful fan speed changes that are less perceptible to the system user.

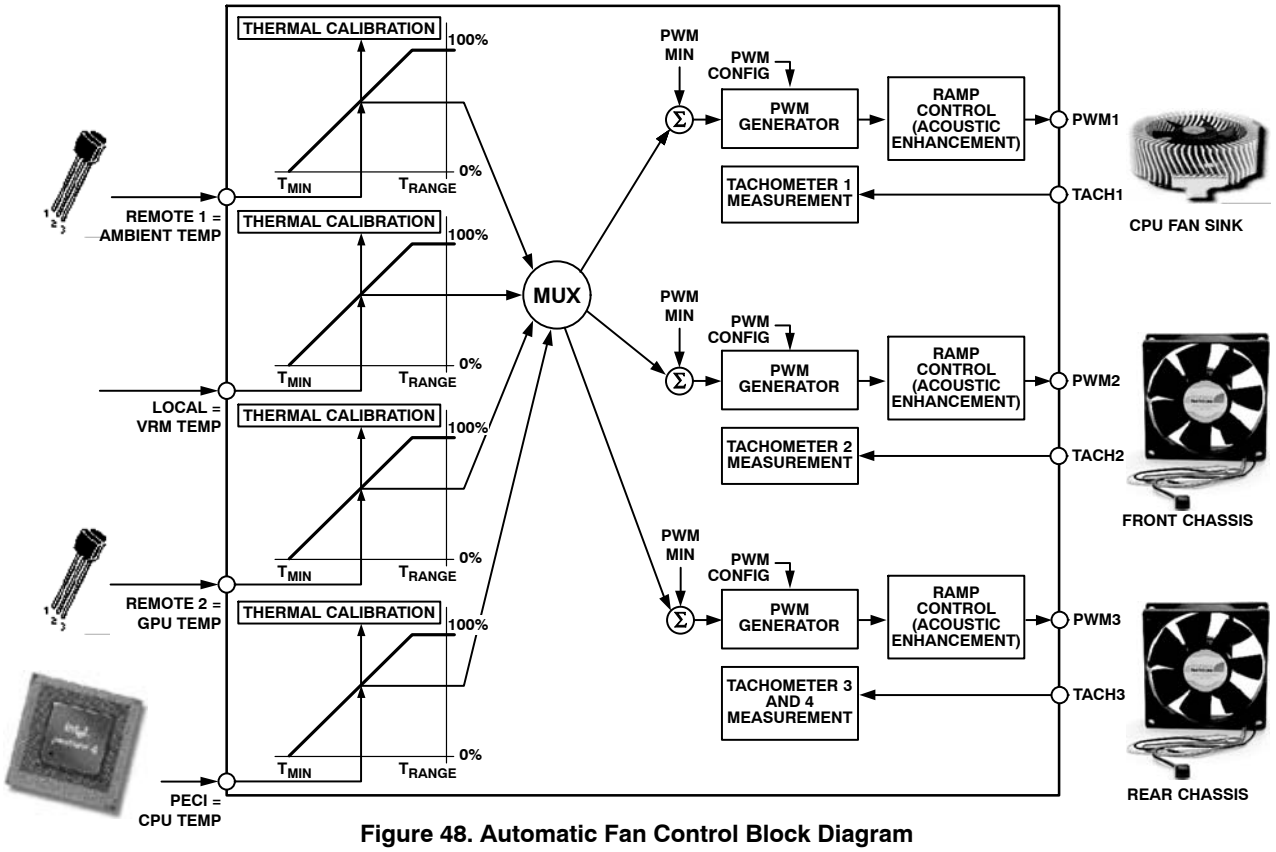


Figure 48. Automatic Fan Control Block Diagram

Step 1: Hardware Configuration

During system design, the motherboard sensing and control capabilities should be addressed early in the design stages. Decisions about how these capabilities are used should involve the system thermal/mechanical engineer. Ask the following questions:

- What ADT7490 functionality is used?
- PWM2 or $\overline{\text{SMBALERT}}$?
- TACH4 fan speed measurement or overtemperature $\overline{\text{THERM}}$ function?
- 2.5 V_{IN} voltage monitoring or overtemperature $\overline{\text{THERM}}$ function?

The ADT7490 offers multifunctional pins that can be reconfigured to suit different system requirements and physical layouts. These multifunction pins are software programmable.

- How many fans are supported in the system, three or four? This influences the choice of whether to use the TACH4 pin or to reconfigure it for the $\overline{\text{THERM}}$ function.
- Is the CPU fan to be controlled using the ADT7490, or will the CPU fan run at full speed 100% of the time?

If run at 100%, it frees up a PWM output, but the system is louder.

- Where is the ADT7490 going to be physically located in the system?

This influences the assignment of the temperature measurement channels to particular system thermal zones. For example, locating the ADT7490 close to the VRM controller circuitry allows the VRM temperature to be monitored using the local temperature channel.

Step 2: Configuring the Muxtiplexer

After the system hardware configuration is determined, the fans can be assigned to particular temperature channels. Not only can fans be assigned to individual channels, but the behavior of the fans is also configurable. For example, fans can be run under automatic fan control, can be run manually (under software control), or can be run at the fastest speed calculated by multiple temperature channels. The mux is the bridge between temperature measurement channels and the three PWM outputs.

Bits [7:5] (BHVR) of Register 0x5C, Register 0x5D, and Register 0x5E (PWM configuration registers) control the behavior of the fans connected to the PWM1, PWM2, and PWM3 outputs, respectively. The values selected for these bits determine how the multiplexer connects a temperature measurement channel to a PWM output.

Automatic Fan Control Multiplexer Options

Bits [7:5] (BHVR), Register 0x5C, Register 0x5D, and Register 0x5E, with the ALT bit (Bit 3) cleared to 0.

000 = Remote 1 temperature controls PWMx
001 = Local temperature controls PWMx
010 = Remote 2 temperature controls PWMx
101 = Fastest speed calculated by local and Remote 2 temperature controls PWMx
110 = Fastest speed calculated by all three temperature channels controls PWMx

The fastest speed calculated options pertain to controlling one PWM output based on multiple temperature channels. The thermal characteristics of the three temperature zones can be set to drive a single fan. An example is the fan turning on when the Remote 1 temperature exceeds 60°C or if the local temperature exceeds 45°C.

Setting the ALT bit in Register 0x5C, Register 0x5D, and Register 0x5E gives alternative behavior settings for Bits [7:5] of the PWM configuration registers.

Bits [7:5] (BHVR), Register 0x5C, Register 0x5D, and Register 0x5E, with the ALT bit (Bit 3) set to 1.

000 = PECI0 reading controls PWMx
001 = PECI1 reading controls PWMx
010 = PECI2 reading controls PWMx
011 = PECI3 reading controls PWMx
101 = Fastest speed calculated by all four PECI readings controls PWMx
111 = Fastest speed calculated by all thermal zones (Local, Rem1, Rem2 and PECI) controls PWMx

Other Mux Options

Bits [7:5] (BHVR), Register 0x5C, Register 0x5D, and Register 0x5E, with the ALT bit (Bit 3) cleared to 0.

011 = PWMx runs full speed
100 = PWMx disabled (default)
111 = Manual mode. PWMx is running under software control. In this mode, PWM duty cycle registers (Register 0x30 to Register 0x32) are writable and control the PWM outputs.

Bits [7:5] (BHVR), Register 0x5C, Register 0x5D, and Register 0x5E, with the ALT bit (Bit 3) set to 1.

100 = PWMx runs at 100% duty cycle
110 = PWMx runs at 100% duty cycle

Step 3: T_{MIN} Settings for Thermal Calibration Channels

T_{MIN} is the temperature at which the fans start to turn on under automatic fan control. The speed at which the fan runs at T_{MIN} is programmed later. The T_{MIN} values chosen are temperature channel specific, for example, 25°C for ambient channel, 30°C for VRM temperature, and 40°C for processor temperature.

T_{MIN} is an 8−bit value, either twos complement or Offset 64, that can be programmed in 1°C increments. A T_{MIN} register is associated with each temperature measurement channel: Remote 1, local, Remote 2 and PECI temperature. When the T_{MIN} value is exceeded, the fan turns on and runs at the minimum PWM duty cycle. The fan turns off once the temperature has dropped below $T_{MIN} - T_{HYST}$.

To overcome fan inertia, the fan is spun up until two valid TACH rising edges are counted. See the Fan Startup Timeout section for more details. In some cases, primarily for psycho−acoustic reasons, it is desirable that the fan never switch off below T_{MIN}. When set, Bits [7:5] of Enhanced Acoustics Register 1 (0x62) keep the fans running at the PWM minimum duty cycle if the temperature should fall below T_{MIN}.

T_{MIN} Registers

Register 0x67, Remote 1 Temperature T_{MIN} = 0x5A (90°C default)

Register 0x68, Local Temperature T_{MIN} = 0x5A (90°C default)

Register 0x69, Remote 2 Temperature T_{MIN} = 0x5A (90°C default)

Register 0x3B, PECI T_{MIN} = 0xE0 (−32°C default)

Enhanced Acoustics Register 1 (Register 0x62)

Bit 7 (MIN3) = 0, PWM3 is off (0% PWM duty cycle) when the temperature is below $T_{MIN} - T_{HYST}$.

Bit 7 (MIN3) = 1, PWM3 runs at PWM3 minimum duty cycle below $T_{MIN} - T_{HYST}$.

Bit 6 (MIN2) = 0, PWM2 is off (0% PWM duty cycle) when the temperature is below $T_{MIN} - T_{HYST}$.

Bit 6 (MIN2) = 1, PWM2 runs at PWM2 minimum duty cycle below $T_{MIN} - T_{HYST}$.

Bit 5 (MIN1) = 0, PWM1 is off (0% PWM duty cycle) when the temperature is below $T_{MIN} - T_{HYST}$.

Bit 5 (MIN1) = 1, PWM1 runs at PWM1 minimum duty cycle below $T_{MIN} - T_{HYST}$.

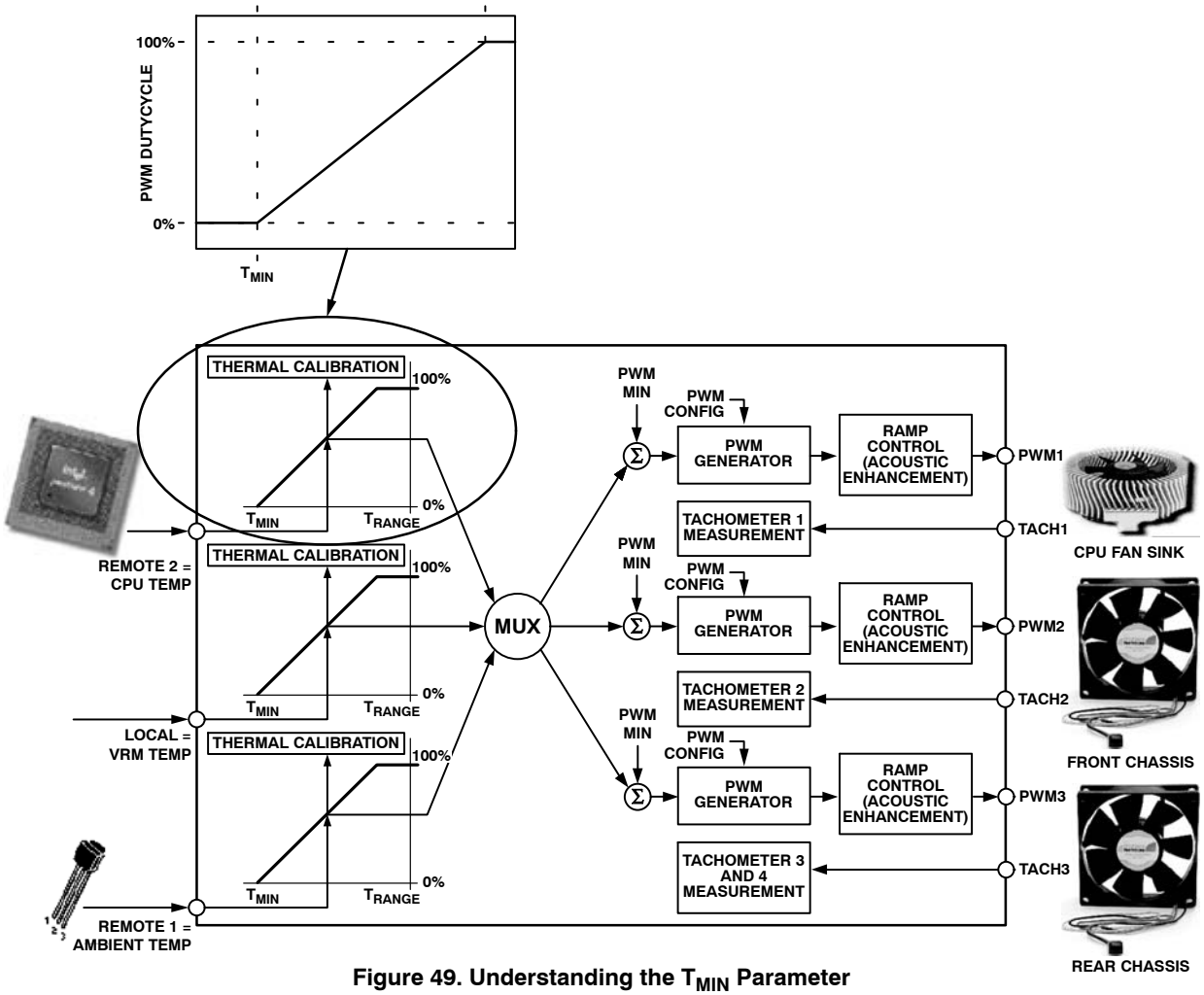


Figure 49. Understanding the T_{MIN} Parameter

Step 4: PWM_{MIN} for Each PWM (Fan) Output

PWM_{MIN} is the minimum PWM duty cycle at which each fan in the system runs. It is also the start speed for each fan under automatic fan control once the temperature rises above T_{MIN}. For maximum system acoustic benefit, PWM_{MIN} should be as low as possible. Depending on the fan used, the PWM_{MIN} setting is usually in the 20% to 33% duty cycle range. This value can be found through fan validation.

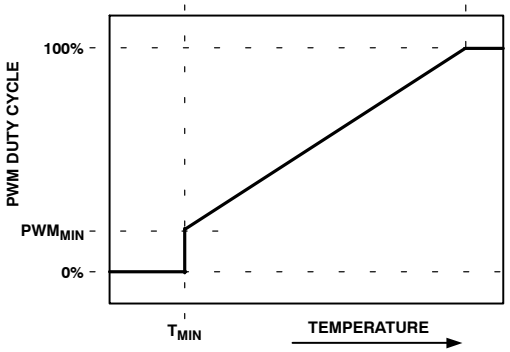


Figure 50. PWM_{MIN} Determines Minimum PWM Duty Cycle

More than one PWM output can be controlled from a single temperature measurement channel. For example, Remote 1 temperature can control PWM1 and PWM2 outputs. If two different fans are used on PWM1 and PWM2, the fan characteristics can be set up differently. As a result, Fan 1 driven by PWM1 can have a different PWM_{MIN} value than that of Fan 2 connected to PWM2. Figure 51 illustrates this as $PWM1_{MIN}$ (front fan) turned on at a minimum duty cycle of 20%, while $PWM2_{MIN}$ (rear fan) is turned on at a minimum of 40% duty cycle. Note that both fans turn on at exactly the same temperature, defined by T_{MIN}.

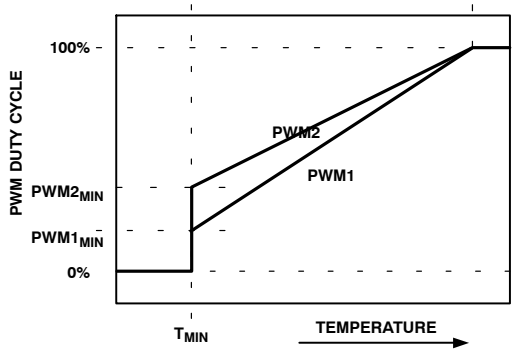


Figure 51. Operating Two Different Fans from a Single Temperature Channel

Programming the PWM_{MIN} Registers

The PWM_{MIN} registers are 8−bit registers that allow the minimum PWM duty cycle for each output to be configured anywhere from 0% to 100%. This allows the minimum PWM duty cycle to be set in steps of 0.39%.

The value to be programmed into the PWM_{MIN} register is given by:

Value (decimal) = PWM_{MIN}/0.39%

Example 1

For a minimum PWM duty cycle of 50%,

Value (decimal) = 50%/0.39% = 128 (decimal)

Value = 128 (decimal) or 0x80 (hexadecimal)

Example 2

For a minimum PWM duty cycle of 33%,

Value (decimal) = 33%/0.39% = 85 (decimal)

Value = 85 (decimal) or 0x54 (hexadecimal)

PWM_{MIN} Registers

Register 0x64, PWM1 Minimum Duty Cycle = 0x80 (50% default)

Register 0x65, PWM2 Minimum Duty Cycle = 0x80 (50% default)

Register 0x66, PWM3 Minimum Duty Cycle = 0x80 (50% default)

Note on Fan Speed and PWM Duty Cycle

The PWM duty cycle does not directly correlate to fan speed in RPM. Running a fan at 33% PWM duty cycle does not equate to running the fan at 33% speed. Driving a fan at 33% PWM duty cycle actually runs the fan at closer to 50% of its full speed. This is because fan speed in %RPM generally relates to the square root of PWM duty cycle. Given a PWM square wave as the drive signal, fan speed in RPM approximates to

$$\%\ \text{fanspeed} = \sqrt{\text{PWM Duty Cycle} \times 10} \qquad \text{(eq. 7)}$$

Step 5: PWM_{MAX} for PWM (Fan) Outputs

PWM_{MAX} is the maximum duty cycle that each fan in the system runs at under the automatic fan speed control loop. For maximum system acoustic benefit, PWM_{MAX} should be as low as possible, but should be capable of maintaining the processor temperature limit at an acceptable level. If the $\overline{\text{THERM}}$ temperature limit is exceeded, the fans are still boosted to 100% for fail−safe cooling.

There is a PWM_{MAX} limit for each fan channel. The default value of this register is 0xFF and has no effect unless it is programmed.

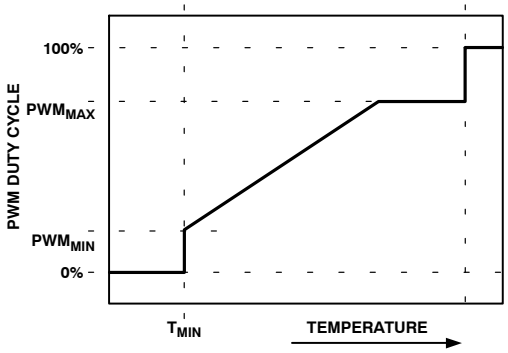


Figure 52. PWM_{MAX} Determines Maximum PWM Duty Cycle Below the $\overline{\text{THERM}}$ Temperature Limit

Programming the PWM_{MAX} Registers

The PWM_{MAX} registers are 8−bit registers that allow the maximum PWM duty cycle for each output to be configured anywhere from 0% to 100%. This allows the maximum PWM duty cycle to be set in steps of 0.39%.

The value to be programmed into the PWM_{MAX} register is given by

Value (decimal) = PWM_{MAX}/0.39%

Example 1

For a maximum PWM duty cycle of 50%,

Value (decimal) – 50%/0.39% = 128 (decimal)

Value = 128 (decimal) or 0x80 (hexadecimal)

Example 2

For a minimum PWM duty cycle of 75%,

Value (decimal) = 75%/0.39% = 85 (decimal)

Value = 192 (decimal) or 0xC0 (hexadecimal)

PWM_{MAX} Registers

Register 0x38, Maximum PWM1 Duty Cycle = 0xFF (100% default)

Register 0x39, Maximum PWM2 Duty Cycle = 0xFF (100% default)

Register 0x3A, Maximum PWM3 Duty Cycle = 0xFF (100% default)

Step 6: T_{RANGE} for Temperature Channels

T_{RANGE} is the range of temperature over which automatic fan control occurs once the programmed T_{MIN} temperature has been exceeded. T_{RANGE} is the temperature range between PWM_{MIN} and 100% PWM where the fan speed changes linearly. Otherwise stated, it is the line drawn between the T_{MIN}/PWM_{MIN} and the (T_{MIN} + T_{RANGE})/100% PWM intersection points.

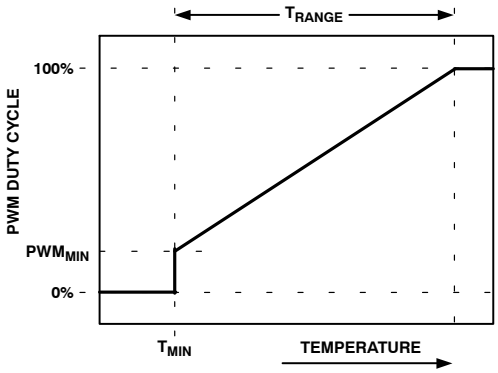


Figure 53. T_{RANGE} Parameter Affects Cooling Slope

The T_{RANGE} is determined by the following procedure:

1. Determine the maximum operating temperature for that channel (for example, 70°C).
2. Determine experimentally the fan speed (PWM duty cycle value) that does not exceed the temperature at the worst−case operating points. For example, 70°C is reached when the fans are running at 50% PWM duty cycle.
3. Determine the slope of the required control loop to meet these requirements.
4. Using the ADT7490 evaluation software, graphically program and visualize this functionality. Ask a local Analog Devices representative for details.

As PWM_{MIN} is changed, the automatic fan control slope changes.

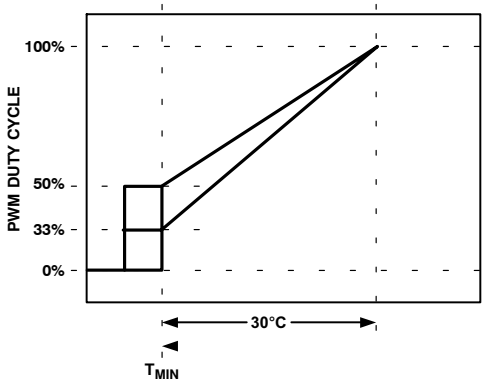


Figure 54. Adjusting PWM_{MIN} Changes the Automatic Fan Control Slope

As T_{RANGE} is changed, the slope changes. As T_{RANGE} gets smaller, the fans reach 100% speed with a smaller temperature change.

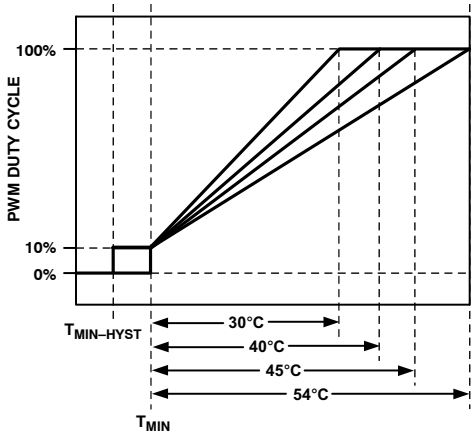


Figure 55. Increasing T_{RANGE} Changes the AFC Slope

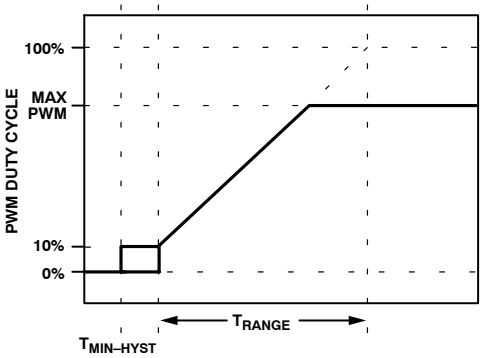


Figure 56. Changing PWM Max Does Not Change the AFC Slope

Selecting T_{RANGE}

The T_{RANGE} value can be selected for each temperature channel: Remote 1, local, Remote 2, and PECI temperature. Bits [7:4] (T_{RANGE}) of Register 0x5F to Register 0x61 and Register 0x3C define the T_{RANGE} value for each temperature channel.

Table 19. Selecting a T_{RANGE} Value

Bits [7:4] (Note 1)	**T_{RANGE} (°C)**
0000	2
0001	2.5
0010	3.33
0011	4
0100	5
0101	6.67
0110	8
0111	10
1000	13.33
1001	16
1010	20
1011	26.67
1100	32 (default)
1101	40
1110	53.33
1111	80

1. Register 0x5F configures Remote 1 T_{RANGE}; Register 0x60 configures local T_{RANGE}; Register 0x61 configures Remote 2 T_{RANGE}, Register 0x3C configures PECI T_{RANGE}.

Actual Changes in PWM Output (Advanced Acoustics Settings)

While the automatic fan control algorithm describes the general response of the PWM output, it is also necessary to note that the enhanced acoustics registers (0x62, 0x63, and 0x3C) can be used to set/clamp the maximum rate of change of PWM output for a given temperature zone. This means that if T_{RANGE} is programmed with an AFC slope that is quite steep, a relatively small change in temperature could cause a large change in PWM output and possibly an audible change in fan speed, which can be noticeable/annoying to end users.

Decreasing the speed of the PWM output changes by programming the smoothing on the appropriate temperature channels (Register 0x62 and Register 0x63) changes how fast the fan speed increases/decreases in the event of a temperature spike. Slowly the PWM duty cycle increases until the PWM duty cycle reaches the appropriate duty cycle as defined by the AFC curve.

Figure 57 shows PWM duty cycle vs. temperature for each T_{RANGE} setting. Figure 57B shows how each T_{RANGE} setting affects fan speed vs. temperature. As can be seen from the graph, the effect on fan speed is nonlinear.

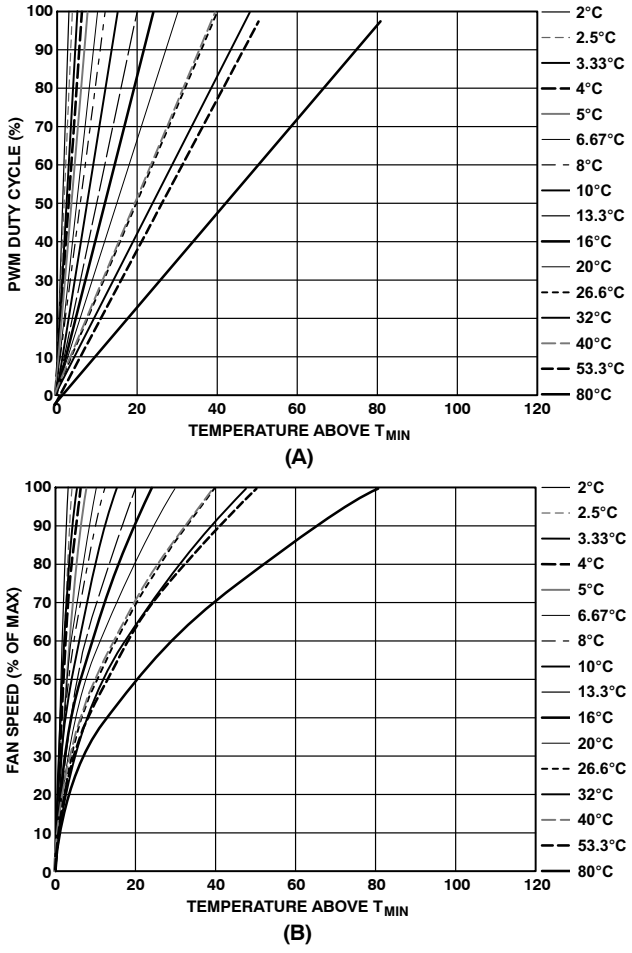


Figure 57. T_{RANGE} vs. Actual Fan Speed (Not PWM Drive) Profile

The graphs in Figure 57 assume the fan starts from 0% PWM duty cycle. Clearly, the minimum PWM duty cycle, PWM_{MIN}, needs to be factored in to see how the loop actually performs in the system. Figure 58 shows how T_{RANGE} is affected when the PWM_{MIN} value is set to 20%. It can be seen that the fan actually runs at about 45% fan speed when the temperature exceeds T_{MIN}.

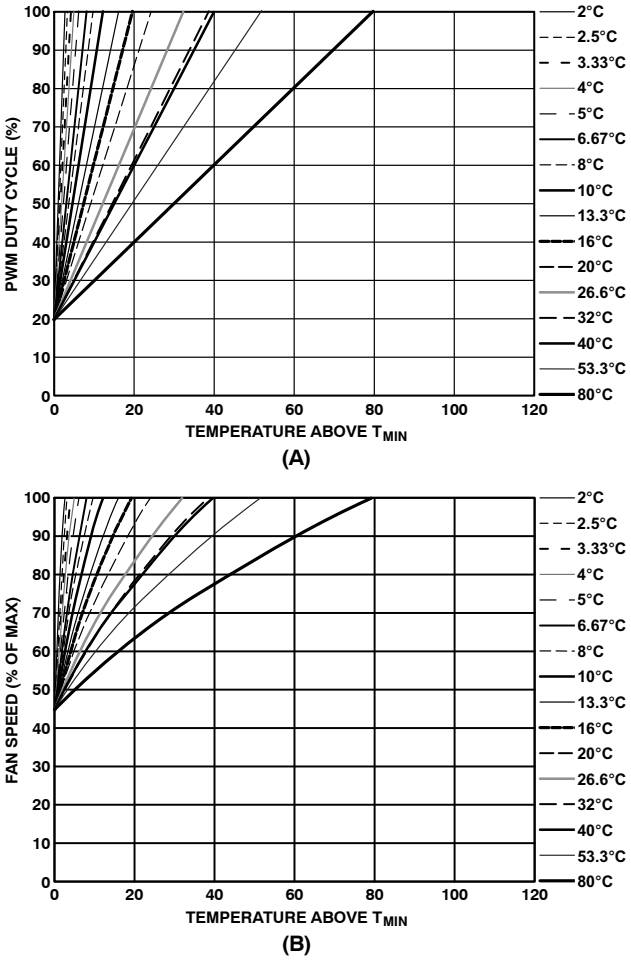


Figure 58. T_{RANGE} and % Fan Speed Slopes with PWM_{MIN} = 20%

Step 7: $T_{\overline{THERM}}$ for Temperature Channels

$T_{\overline{THERM}}$ is the absolute maximum temperature allowed on a temperature channel. For PECI temperature channels, the equivalent parameter is $T_{CONTROL}$. Above this temperature, a component such as the CPU or VRM may be operating beyond its safe operating limit. When the temperature measured exceeds $T_{\overline{THERM}}$, all fans are driven at 100% PWM duty cycle (full speed) to provide critical system cooling.

The fans remain running at 100% until the temperature drops below $T_{\overline{THERM}}$ minus hysteresis, where hysteresis is the number programmed into the hysteresis registers (0x6D and 0x6E). The default hysteresis value is 4°C.

The $T_{\overline{THERM}}$ limit should be considered the maximum worst−case operating temperature of the system. Because

exceeding any $T_{\overline{THERM}}$ limit runs all fans at 100%, it has very negative acoustic effects. Ultimately, this limit should be set up as a fail−safe, and one should ensure that it is not exceeded under normal system operating conditions.

Note that $T_{\overline{THERM}}$ limits are non−maskable and affect the fan speed no matter how automatic fan control settings are configured. This allows some flexibility, because a T_{RANGE} value can be selected based on its slope, while a hard limit (such as 70°C), can be programmed as T_{MAX} (the temperature at which the fan reaches full speed) by setting $T_{\overline{THERM}}$ to that limit (for example, 70°C).

$\overline{THERM}$ Registers

Register 0x6A, Remote 1 $\overline{THERM}$ Temperature Limit = 0x64 (100°C default)

Register 0x6B, Local $\overline{THERM}$ Temperature Limit = 0x64 (100°C default)

Register 0x6C, Remote 2 $\overline{THERM}$ Temperature Limit = 0x64 (100°C default)

Register 0x3D, PECI $T_{CONTROL}$ Limit = 0x00 (0°C default)

$\overline{THERM}$ Hysteresis

$\overline{THERM}$ hysteresis on a particular channel is configured via the hysteresis settings in the following section (0x6D and 0x6E). For example, setting hysteresis on the Remote 1 channel also sets the hysteresis on Remote 1 $\overline{THERM}$.

Hysteresis Registers

Register 0x6D, Remote 1, Local Hysteresis Register

Bits [7:4], Remote 1 Temperature Hysteresis (4°C default)

Bits [3:0], Local Temperature Hysteresis (4°C default)

Register 0x6E, Remote 2, PECI Temperature Hysteresis Register

Bits [7:4], Remote 2 Temperature Hysteresis (4°C default)

Bits [3:0], PECI Temperature Hysteresis (4°C default)

Because each hysteresis setting is four bits, hysteresis values are programmable from 1°C to 15°C. It is not recommended that hysteresis values ever be programmed to 0°C, because this disables hysteresis. In effect, this causes the fans to cycle (during a $\overline{THERM}$ event) between normal speed and 100% speed, or, while operating close to T_{MIN}, between normal speed and off, creating unsettling acoustic noise.

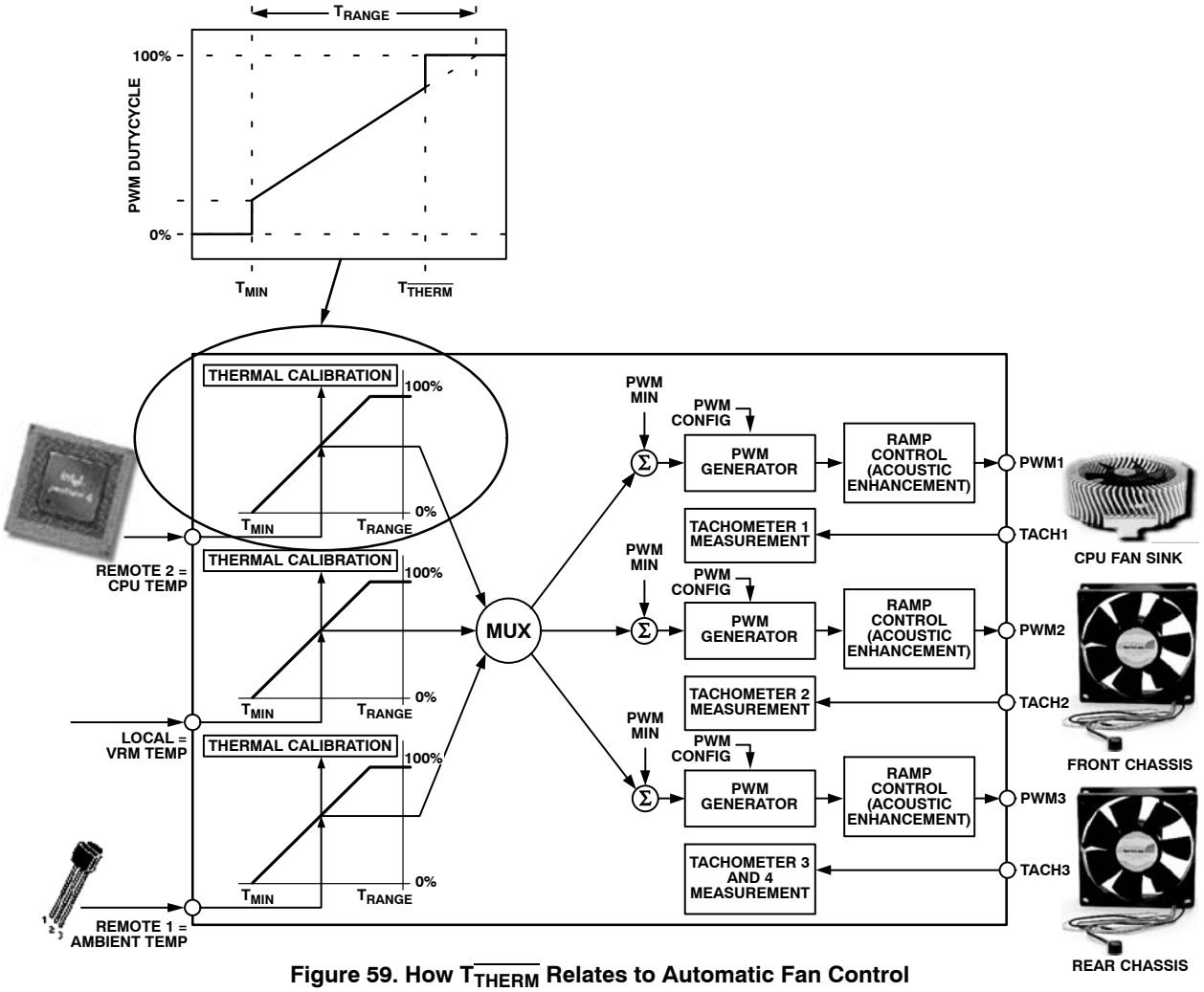


Figure 59. How $T_{\overline{THERM}}$ Relates to Automatic Fan Control

Step 8: T_{HYST} for Temperature Channels

T_{HYST} is the amount of extra cooling a fan provides after the temperature measured has dropped back below T_{MIN} before the fan turns off. The premise for temperature hysteresis (T_{HYST}) is that, without it, the fan would merely chatter, or cycle on and off regularly, whenever the temperature is hovering at about the T_{MIN} setting.

The T_{HYST} value chosen determines the amount of time needed for the system to cool down or heat up as the fan is turning on and off. Values of hysteresis are programmable in the range of 1°C to 15°C. Larger values of T_{HYST} prevent the fans from chattering on and off. The T_{HYST} default value is set at 4°C.

The T_{HYST} setting applies not only to the temperature hysteresis for fan on/off, but the same setting is used for the $T_{\overline{THERM}}$ hysteresis value, described in the Step 7: $T_{\overline{THERM}}$ for Temperature Channels section. Therefore, programming Register 0x6D and Register 0x6E sets the hysteresis for both fan on/off and the $\overline{THERM}$ function.

In some applications, it is required that fans not turn off below T_{MIN}, but remain running at PWM_{MIN}. Bits [7:5] of Enhanced Acoustics Register 1 (0x62) allow the fans to be turned off or to be kept spinning below T_{MIN}. If the fans are always on, the T_{HYST} value has no effect on the fan when the temperature drops below T_{MIN}.

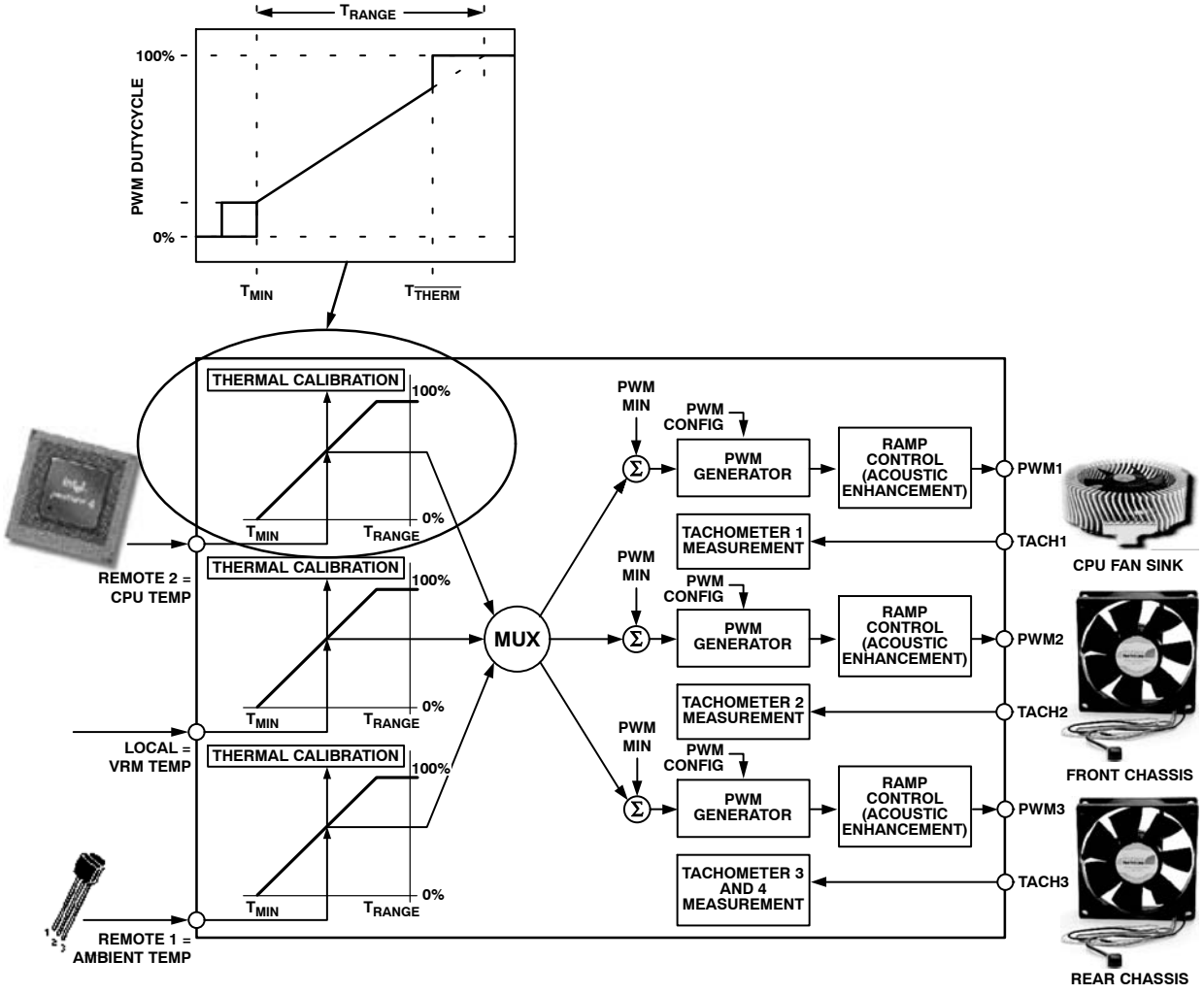


Figure 60. The T_{HYST} Value Applies to Fan On/Off Hysteresis and $\overline{THERM}$ Hysteresis

$\overline{THERM}$ Hysteresis

Any hysteresis programmed via Register 0x6D and Register 0x6E also applies hysteresis on the appropriate $\overline{THERM}$ channel.

Enhanced Acoustics Register 1 (Register 0x62)

Bit 7 (MIN3) = 0, PWM3 is off (0% PWM duty cycle) when temperature is below $T_{MIN} - T_{HYST}$.

Bit 7 (MIN3) = 1, PWM3 runs at PWM3 minimum duty cycle below $T_{MIN} - T_{HYST}$.

Bit 6 (MIN2) = 0, PWM2 is off (0% PWM duty cycle) when the temperature is below $T_{MIN} - T_{HYST}$.

Bit 6 (MIN2) = 1, PWM2 runs at PWM2 minimum duty cycle below $T_{MIN} - T_{HYST}$.

Bit 5 (MIN1) = 0, PWM1 is off (0% PWM duty cycle) when the temperature is below $T_{MIN} - T_{HYST}$.

Bit 5 (MIN1) = 1, PWM1 runs at PWM1 minimum duty cycle below $T_{MIN} - T_{HYST}$.

Configuration Register 6 (Register 0x10)

Bit 0 (SLOW) = 1, slows the ramp rate for PWM changes associated with the Remote 1 temperature channel by 4.

Bit 1 (SLOW) = 1, slows the ramp rate for PWM changes associated with the local temperature channel by 4.

Bit 2 (SLOW) = 1, slows the ramp rate for PWM changes associated with the Remote 2 temperature channel by 4.

Bit 7 (ExtraSlow) = 1, slows the ramp rate for all fans by a factor of 39.2%.

The following sections list the ramp−up times when the SLOW bit is set for each temperature monitoring channel.

Enhanced Acoustics Register 1 (Register 0x62)

Bits [2:0] ACOU, selects the ramp rate for PWM outputs associated with the Remote Temperature 1 input.

000 = 37.5 sec
001 = 18.8 sec
010 = 12.5 sec
011 = 7.5 sec
100 = 4.7 sec
101 = 3.1 sec
110 = 1.6 sec
111 = 0.8 sec

Enhanced Acoustics Register 2 (Register 0x63)

Bits [2:0] ACOU3, selects the ramp rate for PWM outputs associated with the local temperature channel.

000 = 37.5 sec
001 = 18.8 sec
010 = 12.5 sec
011 = 7.5 sec
100 = 4.7 sec
101 = 3.1 sec
110 = 1.6 sec
111 = 0.8 sec

[6:4] ACOU2, selects the ramp rate for PWM outputs associated with the Remote Temperature 2 input.

000 = 37.5 sec
001 = 18.8 sec
010 = 12.5 sec
011 = 7.5 sec
100 = 4.7 sec
101 = 3.1 sec
110 = 1.6 sec
111 = 0.8 sec

When Bit 7 of Configuration Register 6 (0x10) = 1, the preceding ramp rates change to

000 = 52.2 sec
001 = 26.1 sec
010 = 17.4 sec
011 = 10.4 sec
100 = 6.5 sec
101 = 4.4 sec
110 = 2.2 sec
111 = 1.1 sec

Setting the appropriate SLOW Bit 2, Bit 1, or Bit 0 of Configuration Register 6 (0x10) slows the ramp rate further by a factor of 4.

Programming the GPIOs

The ADT7490 has two dedicated GPIOs (Pin 5 and Pin 6).The direction (input or output) and polarity (active high or active low) of the GPIOs is set in the GPIO Configuration Register (0x80). Bit 2 and Bit 3 of Register 0x80 also reflect the state of the GPIO pins when configured as inputs and assert the GPIO pins when configured as outputs.

XNOR Tree Test Mode

The ADT7490 includes an XNOR tree test mode. This mode is useful for in−circuit test equipment at board−level testing. By applying stimulus to the pins included in the XNOR tree, it is possible to detect opens, or shorts, on the system board.

The XNOR tree test is invoked by setting Bit 0 (XEN) of the XNOR Tree Test Enable register (Register 0x6F).

Figure 61 shows the signals that are exercised in the XNOR tree test mode.

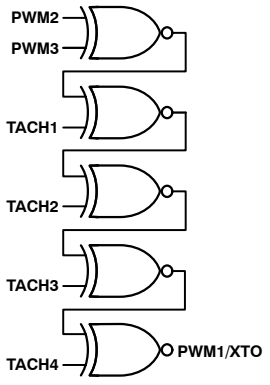


Figure 61. XNOR Tree Test

Register Tables

Table 20. ADT7490 Registers

Addr	R/W	Desc	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	De-fault	Lock-able
0x10	R/W	Config. Reg. 6	Extra Slow	V_{CCP} Low	Res	Res	Res	SLOW Remote 2	SLOW Local	SLOW Remote 1	0x00	Yes
0x11	R/W	Config. Reg. 7	RES	RES	RES	TODIS	FSPDIS	Vx1	FSPD	$\overline{\text{THERM}}$ Hys	0x00	Yes
0x12	R	Extended Revision	RES	RES	RES	RES	RES	RES	RES	–	–	–
0x1A	R	PECI1	7	6	5	4	3	2	1	0	0x80	–
0x1B	R	PECI2	7	6	5	4	3	2	1	0	0x80	–
0x1C	R	PECI3	7	6	5	4	3	2	1	0	0x80	–
0x1D	R	I_{MON} Meas.	9	8	7	6	5	4	3	2	0x00	–
0x1E	R	V_{TT} Meas.	9	8	7	6	5	4	3	2	0x00	–
0x1F	R	Extended Resolution 3	I_{MON}	I_{MON}	V_{TT}	V_{TT}	RES	RES	RES	RES	0x00	–
0x20	R	+2.5V_{IN} Meas.	9	8	7	6	5	4	3	2	0x00	–
0x21	R	V_{CCP} Meas.	9	8	7	6	5	4	3	2	0x00	–
0x22	R	V_{CC} Meas.	9	8	7	6	5	4	3	2	0x00	–
0x23	R	+5V_{IN} Meas.	9	8	7	6	5	4	3	2	0x00	–
0x24	R	+12V_{IN} Meas.	9	8	7	6	5	4	3	2	0x00	–
0x25	R	Remote 1 Temp.	9	8	7	6	5	4	3	2	0x80	–
0x26	R	Local Temp.	9	8	7	6	5	4	3	2	0x80	–
0x27	R	Remote 2 Temp.	9	8	7	6	5	4	3	2	0x80	–
0x28	R	TACH1 Low Byte	7	6	5	4	3	2	1	0	0x00	–
0x29	R	TACH1 High Byte	15	14	13	12	11	10	9	8	0x00	–
0x2A	R	TACH2 Low Byte	7	6	5	4	3	2	1	0	0x00	–
0x2B	R	TACH2 High Byte	15	14	13	12	11	10	9	8	0x00	–
0x2C	R	TACH3 Low Byte	7	6	5	4	3	2	1	0	0x00	–
0x2D	R	TACH3 High Byte	15	14	13	12	11	10	9	8	0x00	–
0x2E	R	TACH4 Low Byte	7	6	5	4	3	2	1	0	0x00	–
0x2F	R	TACH4 High Byte	15	14	13	12	11	10	9	8	0x00	–
0x30	R/W	PWM1 Current Duty Cycle	7	6	5	4	3	2	1	0	0xFF	–
0x31	R/W	PWM2 Current Duty Cycle	7	6	5	4	3	2	1	0	0xFF	–
0x32	R/W	PWM3 Current Duty Cycle	7	6	5	4	3	2	1	0	0xFF	–
0x33	R	PECI0	7	6	5	4	3	2	1	0	0x80	–

Table 20. ADT7490 Registers

Addr	R/W	Desc	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	De-fault	Lock-able
0x34	R/W	PECI Low Limit	7	6	5	4	3	2	1	0	0x81	–
0x35	R/W	PECI High Limit	7	6	5	4	3	2	1	0	0x00	–
0x36	R/W	PECI Config. Register 1	RES	RES	RES	RE–PLACE	DOM0	AVG2	AVG1	AVG0	0x00	Yes
0x38	R/W	Max PWM1 Duty Cycle	7	6	5	4	3	2	1	0	0xFF	Yes
0x39	R/W	Max PWM2 Duty Cycle	7	6	5	4	3	2	1	0	0xFF	Yes
0x3A	R/W	Max PWM3 Duty Cycle	7	6	5	4	3	2	1	0	0xFF	Yes
0x3B	R/W	PECI T_{MIN}	7	6	5	4	3	2	1	0	0xE0	Yes
0x3C	R/W	PECI T_{RANGE}/ Enhanced Acoustics	RANGE	RANGE	RANGE	RANGE	ENP	ACOU	ACOU	ACOU	0xC0	Yes
0x3D	R/W	PECI $T_{CONTROL}$ Limit	7	6	5	4	3	2	1	0	0x00	Yes
0x3E	R	Company ID No.	7	6	5	4	3	2	1	0	0x41	–
0x3F	R	Version	VER3	VER2	VER1	VER0	4–Wire	PECI	REV1	REV0	0x06X	–
0x40	R/W	Config. Register 1	RES	RES	$\overline{\text{THERM}}$ in Manual	PECI Monitor	Fan Boost	RDY	LOCK	STRT	0x04	Yes
0x41	R	Interrupt Status 1	OOL	R2T	LT	R1T	$+5V_{IN}$	V_{CC}	V_{CCP}	$\frac{+2.5V_{IN}}{\overline{\text{THERM}}}$	0x00	–
0x42	R	Interrupt Status 2	D2 FAULT	D1 FAULT	$\frac{\text{FAN4}}{\overline{\text{THERM}}}$	FAN3	FAN2	FAN1	OOL	$+12V_{IN}$	0x00	–
0x43	R	Interrupt Status 3	OOL	RES	RES	RES	OVT ($\overline{\text{THERM}}$ Temp Limit)	COMM	DATA	PECI0	0x00	–
0x44	R/W	$+2.5V_{IN}$ Low Limit	7	6	5	4	3	2	1	0	0x00	–
0x45	R/W	$+2.5V_{IN}$ High Limit	7	6	5	4	3	2	1	0	0xFF	–
0x46	R/W	V_{CCP} Low Limit	7	6	5	4	3	2	1	0	0x00	–
0x47	R/W	V_{CCP} High Limit	7	6	5	4	3	2	1	0	0xFF	–
0x48	R/W	V_{CC} Low Limit	7	6	5	4	3	2	1	0	0x00	–
0x49	R/W	V_{CC} High Limit	7	6	5	4	3	2	1	0	0xFF	–
0x4A	R/W	$+5V_{IN}$ Low Limit	7	6	5	4	3	2	1	0	0x00	–
0x4B	R/W	$+5V_{IN}$ High Limit	7	6	5	4	3	2	1	0	0xFF	–
0x4C	R/W	$+12V_{IN}$ Low Limit	7	6	5	4	3	2	1	0	0x00	–
0x4D	R/W	$+12V_{IN}$ High Limit	7	6	5	4	3	2	1	0	0xFF	–
0x4E	R/W	Remote 1 Temp Low Limit	7	6	5	4	3	2	1	0	0x81	–

Table 20. ADT7490 Registers

Addr	R/W	Desc	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	De-fault	Lock-able
0x4F	R/W	Remote 1 Temp High Limit	7	6	5	4	3	2	1	0	0x7F	–
0x50	R/W	Local Temp Low Limit	7	6	5	4	3	2	1	0	0x81	–
0x51	R/W	Local Temp High Limit	7	6	5	4	3	2	1	0	0x7F	–
0x52	R/W	Remote 2 Temp Low Limit	7	6	5	4	3	2	1	0	0x81	–
0x53	R/W	Remote 2 Temp High Limit	7	6	5	4	3	2	1	0	0x7F	–
0x54	R/W	TACH1 Min Low Byte	7	6	5	4	3	2	1	0	0xFF	–
0x55	R/W	TACH1 Min High Byte	15	14	13	12	11	10	9	8	0xFF	–
0x56	R/W	TACH2 Min Low Byte	7	6	5	4	3	2	1	0	0xFF	–
0x57	R/W	TACH2 Min High Byte	15	14	13	12	11	10	9	8	0xFF	–
0x58	R/W	TACH3 Min Low Byte	7	6	5	4	3	2	1	0	0xFF	–
0x59	R/W	TACH3 Min High Byte	15	14	13	12	11	10	9	8	0xFF	–
0x5A	R/W	TACH4 Min Low Byte	7	6	5	4	3	2	1	0	0xFF	–
0x5B	R/W	TACH4 Min High Byte	15	14	13	12	11	10	9	8	0xFF	–
0x5C	R/W	PWM1 Config. Register	BHVR	BHVR	BHVR	INV	ALT	SPIN	SPIN	SPIN	0x62	Yes
0x5D	R/W	PWM2 Config. Register	BHVR	BHVR	BHVR	INV	ALT	SPIN	SPIN	SPIN	0x62	Yes
0x5E	R/W	PWM3 Config. Register	BHVR	BHVR	BHVR	INV	ALT	SPIN	SPIN	SPIN	0x62	Yes
0x5F	R/W	Remote 1 T_{RANGE}/ PWM1 Frequency	RANGE	RANGE	RANGE	RANGE	HF/LF	FREQ	FREQ	FREQ	0xC4	Yes
0x60	R/W	Local T_{RANGE}/PWM2 Frequency	RANGE	RANGE	RANGE	RANGE	HF/LF	FREQ	FREQ	FREQ	0xC4	Yes
0x61	R/W	Remote 2 T_{RANGE}/PWM3 Frequency	RANGE	RANGE	RANGE	RANGE	HF/LF	FREQ	FREQ	FREQ	0xC4	Yes
0x62	R/W	Enhanced Acoustics Reg. 1	MIN3	MIN2	MIN1	SYNC	EN1	ACOU	ACOU	ACOU	0x00	Yes
0x63	R/W	Enhanced Acoustics Reg. 2	EN2	ACOU2	ACOU2	ACOU2	EN3	ACOU3	ACOU3	ACOU3	0x00	Yes

Table 20. ADT7490 Registers

Addr	R/W	Desc	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	De-fault	Lock-able
0x64	R/W	PWM1 Min Duty Cycle	7	6	5	4	3	2	1	0	0x80	Yes
0x65	R/W	PWM2 Min Duty Cycle	7	6	5	4	3	2	1	0	0x80	Yes
0x66	R/W	PWM3 Min Duty Cycle	7	6	5	4	3	2	1	0	0x80	Yes
0x67	R/W	Remote 1 Temp. T_{MIN}	7	6	5	4	3	2	1	0	0x5A	Yes
0x68	R/W	Local Temp. T_{MIN}	7	6	5	4	3	2	1	0	0x5A	Yes
0x69	R/W	Remote 2 Temp. T_{MIN}	7	6	5	4	3	2	1	0	0x5A	Yes
0x6A	R/W	Remote 1 $\overline{\text{THERM}}$ Temp. Limit	7	6	5	4	3	2	1	0	0x64	Yes
0x6B	R/W	Local $\overline{\text{THERM}}$ Temp. Limit	7	6	5	4	3	2	1	0	0x64	Yes
0x6C	R/W	Remote 2 $\overline{\text{THERM}}$ Temp. Limit	7	6	5	4	3	2	1	0	0x64	Yes
0x6D	R/W	Remote 1 and Local Temp./ T_{MIN} Hysteresis	HYSR1	HYSR1	HYSR1	HYSR1	HYSL	HYSL	HYSL	HYSL	0x44	Yes
0x6E	R/W	Remote 2 and PECI Temp./ T_{MIN} Hysteresis	HYSR2	HYSR2	HYSR2	HYSR2	HYSP	HYSP	HYSP	HYSP	0x44	Yes
0x6F	R/W	XNOR Tree Test Enable	RES	RES	RES	RES	RES	RES	RES	XEN	0x00	Yes
0x70	R/W	Remote 1 Temp Offset	7	6	5	4	3	2	1	0	0x00	Yes
0x71	R/W	Local Temp. Offset	7	6	5	4	3	2	1	0	0x00	Yes
0x72	R/W	Remote 2 Temp. Offset	7	6	5	4	3	2	1	0	0x00	Yes
0x73	R/W	Config. Reg. 2	Shutdown	CONV	ATTN	AVG	Fan3 Detect	Fan2 Detect	Fan1 Detect	Fan PresDT	0x00	Yes
0x74	R/W	Interrupt Mask Reg. 1	OOL	R2T	LT	R1T	$+5V_{IN}$	V_{CC}	V_{CCP}	$\overline{+2.5V_{IN}/\text{THERM}}$	0x00	–
0x75	R/W	Interrupt Mask Reg. 2	D2 FAULT	D1 FAULT	$\overline{\text{FAN4}/\text{THERM}}$	FAN3	FAN2	FAN1	OOL	$+12V_{IN}$/ VC	0x00	–
0x76	R	Extended Resolution 1	$+5V_{IN}$	$+5V_{IN}$	V_{CC}	V_{CC}	V_{CCP}	V_{CCP}	$+2.5V_{IN}$	$+2.5V_{IN}$	0x00	–
0x77	R	Extended Resolution 2	TDM2	TDM2	LTMP	LTMP	TDM1	TDM1	$+12V_{IN}$	$+12V_{IN}$	0x00	–
0x78	R/W	Config. Reg. 3	DC4	DC3	DC2	DC1	FAST	BOOST	$\overline{\text{THERM}}/+2.5V_{IN}$	ALERT Enable	0x00	Yes

Table 20. ADT7490 Registers

Addr	R/W	Desc	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Default	Lockable
0x79	R	$\overline{\text{THERM}}$ Timer Status	TMR	TMR	TMR	TMR	TMR	TMR	TMR	ASRT/ TMR0	0x00	–
0x7A	R/W	$\overline{\text{THERM}}$ Timer Limit	LIMT	LIMT	LIMT	LIMT	LIMT	LIMT	LIMT	LIMT	0x00	–
0x7B	R/W	TACH Pulses per Revolution	FAN4	FAN4	FAN3	FAN3	FAN2	FAN2	FAN1	FAN1	0x55	–
0x7C	R/W	Config. Register 5	R2 $\overline{\text{THERM}}$ Output Only	Local $\overline{\text{THERM}}$ Output Only	R1 $\overline{\text{THERM}}$ Output Only	PECI R1 $\overline{\text{THERM}}$ Output Only	RES	RES	Temp Offset	TWOS COMPL	0x01	Yes
0x7D	R/W	Config. Register 4	BpAtt +12V_{IN}	BpAtt +5V_{IN}	BpAtt V_{CCP}	BpAtt +2.5V_{IN}	Max/Full on $\overline{\text{THERM}}$	$\overline{\text{THERM}}$ Disable	Pin 14 Func	Pin 14 Func	0x00	Yes
0x7E	R	Test 1	Do not write to this register								0x00	Yes
0x7F	R	Test 2	Do not write to this register								0x00	Yes
0x80	R/W	GPIO Config. Register	GPIO1 DIR	GPIO2 DIR	GPIO1 POL	GPIO2 POL	GPIO1	GPIO2	RES	RES	0x00	–
0x81	R	Interrupt Status 4	V_{TT}	I_{MON}	PECI3	PECI2	PECI1	RES	RES	RES	0x00	–
0x82	R/W	Interrupt Mask 3	OOL	RES	RES	RES	OVT	COMM	DATA	PECI0	0x00	–
0x83	R/W	Interrupt Mask 4	V_{TT}	I_{MON}	PECI3	PECI2	PECI1	RES	RES	RES	0x00	–
0x84	R/W	V_{TT} Low Limit	7	6	5	4	3	2	1	0	0x00	Yes
0x85	R/W	I_{MON} Low Limit	7	6	5	4	3	2	1	0	0x00	Yes
0x86	R/W	V_{TT} High Limit	7	6	5	4	3	2	1	0	0xFF	Yes
0x87	R/W	I_{MON} High Limit	7	6	5	4	3	2	1	0	0xFF	Yes
0x88	R/W	PECI Config. 2	#CPU	#CPU	DOM1	DOM2	DOM3	RES	RES	RES	0x00	Yes
0x89	R	TEST 3	Do not write to this register								0x00	Yes
0x8A	R/W	PECI Operating Point	7	6	5	4	3	2	1	0	0xFB	Yes
0x8B	R/W	Remote 1 Operating Point	7	6	5	4	3	2	1	0	0x64	Yes
0x8C	R/W	Local Temp. Operating Point	7	6	5	4	3	2	1	0	0x64	Yes
0x8D	R/W	Remote 2 Operating Point	7	6	5	4	3	2	1	0	0x64	Yes
0x8E	R/W	Dynamic T_{MIN} Control Reg. 1	R2T	LT	R1T	PHTR2	PHTL	PHTR1	V_{CCP}LO	CYR2	0x00	Yes
0x8F	R/W	Dynamic T_{MIN} Control Reg. 2	CYR2	CYR2	CYL	CYL	CYL	CYR1	CYR1	CYR1	0x00	Yes
0x90	R/W	Dynamic T_{MIN} Control Reg. 3	PECI	PHTP	CYP	CYP	CYP	RES	RES	RES	0x00	Yes

Table 20. ADT7490 Registers

Addr	R/W	Desc	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	De-fault	Lock-able
0x94	R/W	PECI0 Temp. Offset	7	6	5	4	3	2	1	0	0x00	Yes
0x95	R/W	PECI1 Temp. Offset	7	6	5	4	3	2	1	0	0x00	Yes
0x96	R/W	PECI2 Temp. Offset	7	6	5	4	3	2	1	0	0x00	Yes
0x97	R/W	PECI3 Temp. Offset	7	6	5	4	3	2	1	0	0x00	Yes
–	0x41	–	–	0x74	OOL	R2T	LT	R1T	$+5V_{IN}$	V_{CC}	V_{CCP}	$+2.5V_{IN}$/ $\overline{THERM}$

Table 21. Register 0x10 — Configuration Register 6 (Power−On Default = 0x00)

Bit No.	Mnemonic	R/W (Note 1)	Description
[0]	SLOW Remote 1	R/W	When this bit is set, fan smoothing times are multiplied x4 for Remote 1 temperature channel (as defined in Register 0x62).
[1]	SLOW Local	R/W	When this bit is set, fan smoothing times are multiplied x4 for local temperature channel (as defined in Register 0x63).
[2]	SLOW Remote 2	R/W	When this bit is set, fan smoothing times are multiplied x4 for Remote 2 temperature channel (as defined in Register 0x63).
[3]	Res	N/A	Reserved.
[4]	Res	N/A	Reserved.
[5]	Res	N/A	Reserved.
[6]	V_{CCP} Low	R/W	V_{CCP} Low = 1. When the power is supplied from 3.3 V STANDBY and the core voltage (V_{CCP}) drops below its V_{CCP} low limit value (Register 0x46), the following occurs: Status Bit 1 in Status Register 1 is set. $\overline{SMBALERT}$ is generated, if enabled. $\overline{PROCHOT}$ monitoring is disabled. Everything is re−enabled once V_{CCP} increases above the V_{CCP} low limit. When V_{CCP} increases above the low limit: $\overline{PROCHOT}$ monitoring is enabled. Fans return to their programmed state after a spin−up cycle.
[7]	ExtraSlow	R/W	When this bit is set, all fan smoothing times are increased by a further 39.2%

1. This register becomes read-only when the Configuration Register 1 (0x40) LOCK bit is set to 1. Any subsequent attempts to write to this register fail.

Table 22. Register 0x11 — Configuration Register 7 (Power−On Default = 0x00)

Bit No.	Mnemonic	R/W (Note 1)	Description
[0]	THERMHys	R/W	$\overline{THERM}$ hysteresis is enabled by default. Setting this bit to 1 disables $\overline{THERM}$ hysteresis.
[1]	FSPD	R/W	When set to 1, this bit runs all fans at maximum speed as programmed in the maximum PWM duty cycle registers (0x38 to 0x3A). Power−on default = 0. This bit is not locked at any time.
[2]	Vx1	R/W	BIOS should set this bit to 1 when the ADT7490 is configured to measure current from an Analog Devices ADOPT VRM controller and to measure the CPU core voltage. This bit allows monitoring software to display CPU watts usage. (Lockable.)
[3]	FSPDIS	R/W	Logic 1 disables fan spin−up for two TACH pulses. Instead, the PWM outputs go high for the entire fan spin−up timeout selected.
[4]	TODIS	R/W	When this bit is set to 1, the SMBus timeout feature is disabled. In this state, if at any point during an SMBus transaction involving the ADT7490 activity ceases for more than 35 ms, the ADT7490 assumes the bus is locked and releases the bus. This allows the ADT7490 to be used with SMBus controllers that cannot handle SMBus timeouts. (Lockable.)
[7:5]	RES	N/A	Reserved. Do not write to these bits.

1. This register becomes read-only when the Configuration Register 1 (0x40) LOCK bit is set to 1. Any subsequent attempts to write to this register fail.

Table 23. PECI Reading Registers (Power−On Default = 0x80)

Register Address	R/W	Description
0x33	Read−only	PECI0: This register reads the eight bits representative of PECI Client Address 0x30.
0x1A	Read−only	PECI1: This register reads the eight bits representative of PECI Client Address 0x31.
0x1B	Read−only	PECI2: This register reads the eight bits representative of PECI Client Address 0x32.
0x1C	Read−only	PECI3: This register reads the eight bits representative of PECI Client Address 0x33.

Table 24. I_{MON}/V_{TT} Reading Registers (Power−On Default = 0x00)

Register Address	R/W	Description
0x1D	Read−only	Reflects the voltage measurement at the I_{MON} input on Pin 19 (8 MSBs of reading). Input range of 0 V to 2.25 V.
0x1E	Read−only	Reflects the voltage measurement at the V_{TT} input on Pin 8 (8 MSBs of reading). Input range of 0 V to 2.25 V.

Table 25. Register 0x1F — Extended Resolution 3 (Power−On Default = 0x00)

Bit No.	R/W	Description
[3:0]	Read−only	Reserved.
[5:4]	Read−only	Hold the two LSBs of the 10−bit V_{TT} measurement.
[7:6]	Read−only	Hold the two LSBs of the 10−bit I_{MON} measurement.

Table 26. Voltage Reading Registers (Power−On Default = 0x00) (Note 1)

Register Address	R/W	Description
0x20	Read−only	Reflects the voltage measurement at the 2.5 V_{IN} input on Pin 22 (8 MSBs of reading).
0x21	Read−only	Reflects the voltage measurement (Note 2) at the V_{CCP} input on Pin 23 (8 MSBs of reading).
0x22	Read−only	Reflects the voltage measurement (Note 3) at the V_{CC} input on Pin 4 (8 MSBs of reading).
0x23	Read−only	Reflects the voltage measurement at the 5 V_{IN} input on Pin 20 (8 MSBs of reading).
0x24	Read−only	Reflects the voltage measurement at the 12 V_{IN} input on Pin 21 (8 MSBs of reading).

1. If the extended resolution bits of these readings are also being read, the extended resolution registers (Register 0x76, Register 0x77) must be read first. Once the extended resolution registers have been read, the associated MSB reading registers are frozen until read. Both the extended resolution registers and the MSB registers are frozen.
2. If V_{CCP} Low (Bit 6 of 0x10) is set, V_{CCP} can control the sleep state of the ADT7490.
3. V_{CC} (Pin 4) is the supply voltage for the ADT7490.

Table 27. Temperature Reading Registers (Power−On Default = 0x80) (Note 1 and 2)

Register Address	R/W	Description
0x25	Read−only	Remote 1 temperature reading (Note 3 and 4) (8 MSBs of reading).
0x26	Read−only	Local temperature reading (8 MSBs of reading).
0x27	Read−only	Remote 2 temperature reading (Note 3 and 4) (8 MSBs of reading).

1. If the extended resolution bits of these readings are also being read, the extended resolution registers (Register 0x76, Register 0x77) must be read first. Once the extended resolution registers have been read, all associated MSB reading registers are frozen until read. Both the extended resolution registers and the MSB registers are frozen.
2. These temperature readings can be in twos complement or Offset 64 format; this interpretation is determined by Bit 0 of Configuration Register 5 (0x7C).
3. In twos complement mode, a temperature reading of −128°C (0x80) indicates a diode fault (open or short) on that channel.
4. In Offset 64 mode, a temperature reading of −64°C (0x00) indicates a diode fault (open or short) on that channel.

Table 28. Fan Tachometer Reading Registers (Power−On Default = 0x00) (Note 1)

Register Address	R/W	Description
0x28	Read−only	TACH1 low byte.
0x29	Read−only	TACH1 high byte.
0x2A	Read−only	TACH2 low byte.
0x2B	Read−only	TACH2 high byte.
0x2C	Read−only	TACH3 low byte.
0x2D	Read−only	TACH3 high byte.
0x2E	Read−only	TACH4 low byte.
0x2F	Read−only	TACH4 high byte.

1. These registers count the number of 11.11 μs periods (based on an internal 90 kHz clock) that occur between a number of consecutive fan TACH pulses (default = 2). The number of TACH pulses used to count can be changed using the TACH Pulses per Revolution register (Register 0x7B). This allows the fan speed to be accurately measured. Because a valid fan tachometer reading requires that two bytes be read, the low byte must be read first. Both the low and high bytes are then frozen until read. At power-on, these registers contain 0x0000 until the first valid fan TACH measurement is read into these registers. This prevents false interrupts from occurring while the fans are spinning up. A count of 0xFFFF indicates that a fan is one of the following: stalled or blocked (object jamming the fan), failed (internal circuitry destroyed), or not populated. (The ADT7490 expects to see a fan connected to each TACH. If a fan is not connected to that TACH, its TACH minimum high and low bytes should be set to 0xFFFF.) An alternate function, for example, is TACH4 reconfigured as the $\overline{\text{THERM}}$ pin.

Table 29. Current PWM Duty Cycle Registers (Power−On Default = 0xFF) (Note 1)

Register Address	R/W	Description
0x30	R/W	PWM1 current duty cycle (0% to 100% duty cycle = 0x00 to 0xFF).
0x31	R/W	PWM2 current duty cycle (0% to 100% duty cycle = 0x00 to 0xFF).
0x32	R/W	PWM3 current duty cycle (0% to 100% duty cycle = 0x00 to 0xFF).

1. These registers reflect the PWM duty cycle driving each fan at any given time. When in automatic fan speed control mode, the ADT7490 reports the PWM duty cycles back through these registers. The PWM duty cycle values vary according to temperature in automatic fan speed control mode. During fan startup, these registers report back 0x00. In manual mode, the PWM duty cycle outputs can be set to any duty cycle value by writing to these registers.

Table 30. Register 0x33 — PECI0 Reading Register (Power−On Default = 0x80)

Register Address	R/W	Description
0x33	Read−only	PECI0: This register reads the eight bits representative of PECI Client Address 0x30.

Table 31. PECI Limit Registers

Register Address	R/W	Description	Power−On Default
0x34	R/W	PECI low limit.	0x81
0x35	R/W	PECI high limit.	0x00

Table 32. Register 0x36 — PECI Configuration Register 1 (Power−On Default = 0x00)

Bit No.	Mnemonic	R/W (Note 1)	Description
[2:0]	AVG[2:0]	R/W	PECI Smoothing Interval. These bits set the duration over which smoothing is carried out on the PECI data read. Note that the PECI smoothing interval is equal to the PECI register update interval. The smoothing interval is calculated using the following formula: Smooth Interval = #reads x (t_{BIT} x 67 x #CPU + t_{IDLE}) where: #reads is the number of readings defined below. t_{BIT} is the negotiated bit rate. 67 is the number of bits in each PECI reading. #CPU is the number of CPUs providing PECI data (1 to 4). t_{IDLE} = 14 μs, the delay between consecutive reads.
			Bit Code / **Number of PECI Readings** 000 / 16 001 / 2048 010 / 4096 011 / 8192 100 / 16384 101 / 32768 110 / 65536 111 / Reserved
[3]	DOM0	R/W	CPU Domain Count information. Set to 0 indicates that CPU 1 associated with the PECI0 reading has a single domain (default). Set to 1 indicates that the system CPU 1 contains two domains.
[4]	REPLACE	R/W	If this bit is set to 0, it indicates that the ADT7490 is operating in standard mode. If this bit is set to 1, the Remote 1 Temperature register (Register 0x25) is overwritten by PECI0 information (Register 0x33) and vice versa. Note that in this mode, all associated user programmable limit and fan control registers are also swapped and should be programmed in the appropriate PECI or absolute temperature format.
[7:5]	RES	R	Reserved.

1. These registers become read-only when the Configuration Register 1 (0x40) LOCK bit is set to 1. Any subsequent attempts to write to these registers fail.

Table 33. Maximum PWM Duty Cycle (Power−On Default = 0xFF) (Note 1)

Register Address	R/W (Note 2)	Description
0x38	R/W	Maximum duty cycle for PWM1 output, default = 100% (0xFF).
0x39	R/W	Maximum duty cycle for PWM2 output, default = 100% (0xFF).
0x3A	R/W	Maximum duty cycle for PWM3 output, default = 100% (0xFF).

1. These registers set the maximum PWM duty cycle of the PWM output.
2. These registers become read-only when the Configuration Register 1 (0x40) LOCK bit is set to 1. Any subsequent attempts to write to these registers fail.

Table 34. PECI T_{MIN} Register (Power−On Default = 0xE0, Value = −32)

Register Address	R/W (Note 1)	Description
0x3B	R/W	PECI T_{MIN}. When the PECI measurement exceeds PECI T_{MIN}, the appropriate fans run at PWM_{MIN} and increase according to the automatic fan speed control slope.

1. This register becomes read-only when the Configuration Register 1 (0x40) LOCK bit is set. Any further attempts to write to this register have no effect.

Table 35. Register 0x3C — PECI T_{RANGE}/Enhanced Acoustics Register (Power−On Default = 0xC0)

Bit No.	Mnemonic	R/W (Note 1)	Description	
[2:0]	ACOU	R/W	Assuming that PWMx is associated with the PECI channel, these bits define the maximum rate of change of the PWMx output for PECI temperature−related changes. Instead of the fan speed jumping instantaneously to its newly determined speed, it ramps gracefully at the rate determined by these bits. This feature ultimately enhances the acoustics of the fan. The smoothing times below are based on a refresh rate of the round robin cycle. The PECI data, for 0% to 100%, must be multiplied each time by: PECI Refresh Rate / Round Robin Cycle where the PECI refresh rate is defined in Register 0x36 and the round robin cycle is typically 165 ms.	
			When Bit 7 of Configuration Register 6 (0x10) is 0	
			Bit Code	**Time for 0% to 100%**
			000 = 1 001 = 2 010 = 3 011 = 4 100 = 8 101 = 12 110 = 24 111 = 48	37.5 sec 18.8 sec 12.5 sec 7.5 sec 4.7 sec 3.1 sec 1.6 sec 0.8 sec
[2:0]	ACOU	R/W	**When Bit 7 of Configuration Register 6 (0x10) is 1**	
			Bit Code	**Time for 0% to 100%**
			000 = 1 001 = 2 010 = 3 011 = 4 100 = 8 101 = 12 110 = 24 111 = 48	52.2 sec 26.1 sec 17.4 sec 10.4 sec 6.5 sec 4.4 sec 2.2 sec 1.1 sec
[3]	ENP	R/W	When this bit is set to 1, smoothing is enabled on the PECI channel allowing enhanced acoustics on the associated PWM output.	
[7:4]	RANGE	R/W	These bits determine the PWM duty cycle vs. the temperature range for automatic fan control.	
			Bit Code	**Temperature**
			0000 0001 0010 0011 0100 0101 0110 0111 1000 1001 1010 1011 1100 1101 1110 1111	2°C 2.5°C 3.33°C 4°C 5°C 6.67°C 8°C 10°C 13.33°C 16°C 20°C 26.67°C 32°C (default) 40°C 53.33°C 80°C

1. This register becomes read-only when the Configuration Register 1 (0x40) LOCK bit is set to 1. Any subsequent attempts to write to this register fail.

Table 36. $T_{CONTROL}$ Limit Register (Power−On Default = 0x00) (Note 1)

Register Address	R/W (Note 2)	Description
0x3D	R/W	PECI $T_{CONTROL}$ limit.

1. If any PECI reading exceeds the $T_{CONTROL}$ limit, all PWM outputs drive their fans at 100% duty cycle. This is a fail-safe mechanism incorporated to cool the system in the event of a critical overtemperature. It also ensures some level of cooling in the event that software or hardware locks up. If set to 0x80, this feature is disabled. The PWM output remains at 100% until the temperature drops below $T_{CONTROL}$ limit − hysteresis.
2. This register becomes read-only when the Configuration Register 1 (0x40) LOCK bit is set to 1. Any further attempts to write to this register have no effect.

Table 37. Register 0x3F — Version Register

Bit No.	Mnemonic	R/W	Description
[1:0]	REV[1:0]	Read−only	These two bits indicate the ADT7490 silicon revision number. 0x00 indicates Revision 0, 0x01 indicates Revision 1, and so on. 0x11 indicates that further revision information can be found in the “Extended Revision” register (0x12). The revision number is then found by adding 0x11 to the contents of the extended revision register.
[2]	PECI	Read−only	This bit is set to 1 indicating that the ADT7490 supports the PECI interface.
[3]	4−Wire	Read−only	This bit is set to 1 indicating that the ADT7490 may be configured to drive 4−wire fans using high frequency PWM.
[7:4]	VER[3:0]	Read−only	These bits indicate the version number of the device. This is set to 6, indicating that the ADT7490 is part of the Heceta 6 ASIC family.

Table 38. Register 0x40 — Configuration Register 1 (Power−On Default = 0x04)

Bit No.	Mnemonic	R/W (Note 1)	Description
[0]	STRT (Notes 2, 3)	R/W	Logic 1 enables monitoring and PWM control outputs based on the limit settings programmed. Logic 0 disables monitoring and PWM control is based on the default powerup limit settings. Note that the limit values programmed are preserved even if a Logic 0 is written to this bit and the default settings are enabled. This bit does not become locked once Bit 1 (LOCK bit) is set.
[1]	LOCK	Write once	Logic 1 locks all limit values to their current settings. Once this bit is set, all lockable registers become read−only and cannot be modified until the ADT7490 is powered down and powered up again. This prevents rogue programs such as viruses from modifying critical system limit settings. (Lockable.)
[2]	RDY	Read−only	This bit is set to 1 by the ADT7490 to indicate that the device is fully powered up and ready to begin system monitoring.
[3]	Fan Boost	R/W	When this bit is set to Logic 1, all PWM outputs go to 100% regardless of other fan speed configurations and automatic fan speed control settings. When this bit is set to 0, the fan speed control returns to the fan speed setting calculated by the preprogrammed fan speed control settings. This bit remains writable after the LOCK bit is set.
[4]	PECI Monitor	R/W	Set this bit to Logic 1 to enable CPU thermal monitoring via PECI interface. This bit becomes read−only when the LOCK bit is set.
[5]	$\overline{\text{THERM}}$ in Manual	R/W	When this bit is set to Logic 1, $\overline{\text{THERM}}$ is enabled so that the fans go to 100% duty cycle on a $\overline{\text{THERM}}$ or $T_{CONTROL}$ assertion overriding any other fan setting, even when the PWMs are configured for manual mode, or disabled. This bit becomes read−only when the LOCK bit is set.
[7:6]	RES	Read−only	Reserved.

1. This register becomes read-only when the Configuration Register 1 (0x40) LOCK bit is set to 1. Any subsequent attempts to write to this register fail.
2. Bit 0 (STRT) of Configuration Register 1 (0x40) remains writable after the LOCK bit is set.
3. When monitoring (STRT) is disabled, PWM outputs always go to 100% for thermal protection.

Table 39. Register 0x41 — Interrupt Status Register 1 (Power−On Default = 0x00)

Bit No.	Mnemonic	R/W	Description
[0]	+2.5 V_{IN}/ $\overline{THERM}$	Read−only	+2.5 V_{IN} = 1 indicates that the 2.5 V_{IN} high or low limit has been exceeded. This bit is cleared on a read of the status register only if the error condition has subsided. If Pin 22 is configured as $\overline{THERM}$, this bit is asserted when the timer limit has been exceeded.
[1]	V_{CCP}	Read−only	V_{CCP} = 1 indicates that the V_{CCP} high or low limit has been exceeded. This bit is cleared on a read of the status register only if the error condition has subsided.
[2]	V_{CC}	Read−only	V_{CC} = 1 indicates that the V_{CC} high or low limit has been exceeded. This bit is cleared on a read of the status register only if the error condition has subsided.
[3]	+5 V_{IN}	Read−only	+5 V_{IN} = 1 indicates that the 5 V_{IN} high or low limit has been exceeded. This bit is cleared on a read of the status register only if the error condition has subsided.
[4]	R1T	Read−only	R1T = 1 indicates that the Remote 1 low or high temperature has been exceeded. This bit is cleared on a read of the status register only if the error condition has subsided.
[5]	LT	Read−only	LT = 1 indicates that the local low or high temperature has been exceeded. This bit is cleared on a read of the status register only if the error condition has subsided.
[6]	R2T	Read−only	R2T = 1 indicates that the Remote 2 low or high temperature has been exceeded. This bit is cleared on a read of the status register only if the error condition has subsided.
[7]	OOL	Read−only	OOL = 1 indicates that an out−of−limit event has been latched in Interrupt Status Register 2 (0x42). This bit is a logical OR of all status bits in Interrupt Status Register 2. Software can test this bit in isolation to determine whether any of the voltage, temperature, or fan speed readings represented by Interrupt Status Register 2 are out−of−limit, which eliminates the need to read Interrupt Status Register 2 during every interrupt or polling cycle.

Table 40. Register 0x42 — Interrupt Status Register 2 (Power−On Default = 0x00)

Bit No.	Mnemonic	R/W	Description
[0]	+12 V_{IN}	Read−only	+12 V_{IN} = 1 indicates that the 12 V_{IN} high or low limit has been exceeded. This bit is cleared on a read of the status register only if the error condition has subsided.
[1]	OOL	Read−only	OOL = 1 indicates that an out−of−limit event has been latched in Interrupt Status Register 3 (0x43). This bit is a logical OR of all status bits in Interrupt Status Register 3. Software can test this bit in isolation to determine whether any of the voltage, temperature, or fan speed readings represented by Interrupt Status Register 3 are out−of−limit, which eliminates the need to read Interrupt Status Register 3 during every interrupt or polling cycle.
[2]	FAN1	Read−only	FAN1 = 1 indicates that Fan 1 has dropped below minimum speed or has stalled. This bit is not set when the PWM1 output is off.
[3]	FAN2	Read−only	FAN2 = 1 indicates that Fan 2 has dropped below minimum speed or has stalled. This bit is not set when the PWM2 output is off.
[4]	FAN3	Read−only	FAN3 = 1 indicates that Fan 3 has dropped below minimum speed or has stalled. This bit is not set when the PWM3 output is off.
[5]	FAN4/ $\overline{THERM}$	Read−only	When Pin 14 is programmed as a TACH4 input, FAN4 = 1 indicates that Fan 4 has dropped below minimum speed or has stalled. This bit is not set when the PWM3 output is off. If Pin 14 is configured as the $\overline{THERM}$ timer input for $\overline{THERM}$ monitoring, this bit is set when the $\overline{THERM}$ assertion time exceeds the limit programmed in the $\overline{THERM}$ timer limit register (Register 0x7A).
[6]	D1 FAULT	Read−only	D1 FAULT = 1 indicates either an open or short circuit on the Thermal Diode 1 inputs.
[7]	D2 FAULT	Read−only	D2 FAULT = 1 indicates either an open or short circuit on the Thermal Diode 2 inputs.

Table 41. Register 0x43 — Interrupt Status Register 3 (Power−On Default = 0x00)

Bit No.	Mnemonic	R/W	Description
[0]	PECI0	Read−only	A Logic 1 indicates that the PECI high or low limit has been exceeded by the PECI value from PECI Client Address 0x30. This bit is cleared on a read of the status register only if the error condition has subsided.
[1]	DATA	Read−only	A Logic 1 indicates that valid PECI data cannot be obtained for the processor and a specified error code has been recorded.
[2]	COMM	Read−only	A Logic 1 indicates that there is a communications error (for example, invalid FCS) on the PECI interface.
[3]	OVT ($\overline{\text{THERM}}$ Temp Limit)	Read−only	OVT = 1 indicates that one of the $\overline{\text{THERM}}$ overtemperature limits has been exceeded. This bit is cleared on a read of the status register when the temperature drops below $\overline{\text{THERM}}$ − T_{HYST}.
[6:4]	RES	Read−only	Reserved.
[7]	OOL	Read−only	OOL = 1 indicates that an out−of−limit event has been latched in Interrupt Status Register 4 (0x81). This bit is a logical OR of all status bits in Interrupt Status Register 4. Software can test this bit in isolation to determine whether any of the voltage, temperature, or fan speed readings represented by Interrupt Status Register 4 are out−of−limit, which eliminates the need to read Interrupt Status Register 4 during every interrupt or polling cycle.

Table 42. Voltage Limit Registers (Note 1)

Register Address	R/W	Description (Note 2)	Power−On Default
0x44	R/W	+2.5 V_{IN} low limit.	0x00
0x45	R/W	+2.5 V_{IN} high limit.	0xFF
0x46	R/W	V_{CCP} low limit.	0x00
0x47	R/W	V_{CCP} high limit.	0xFF
0x48	R/W	V_{CC} low limit.	0x00
0x49	R/W	V_{CC} high limit.	0xFF
0x4A	R/W	+5 V_{IN} low limit.	0x00
0x4B	R/W	+5 V_{IN} high limit.	0xFF
0x4C	R/W	+12 V_{IN} low limit.	0x00
0x4D	R/W	+12 V_{IN} high limit.	0xFF

1. Setting the Configuration Register 1 (0x40) LOCK bit has no effect on these registers.
2. High limits: An interrupt is generated when a value exceeds its high limit (> comparison). Low limits: An interrupt is generated when a value is equal to or below its low limit (≤ comparison).

Table 43. Temperature Limit Registers (Note 1)

Register Address	R/W	Description (Note 2)	Power−On Default
0x4E	R/W	Remote 1 temperature low limit.	0x81
0x4F	R/W	Remote 1 temperature high limit.	0x7F
0x50	R/W	Local temperature low limit.	0x81
0x51	R/W	Local temperature high limit.	0x7F
0x52	R/W	Remote 2 temperature low limit.	0x81
0x53	R/W	Remote 2 temperature high limit.	0x7F

1. Exceeding any of these temperature limits by 1°C causes the appropriate status bit to be set in the interrupt status register. Setting the Configuration Register 1 (0x40) LOCK bit has no effect on these registers.
2. High limits: An interrupt is generated when a value exceeds its high limit (> comparison). Low limits: An interrupt is generated when a value is equal to or below its low limit (≤ comparison).

Table 44. Fan Tachometer Limit Registers (Note 1)

Register Address	R/W	Description	Power−On Default
0x34	R/W	PECI low limit.	0x81
0x54	R/W	TACH1 minimum low byte.	0xFF
0x55	R/W	TACH1 minimum high byte/single−channel ADC channel select.	0xFF
0x56	R/W	TACH2 minimum low byte.	0xFF
0x57	R/W	TACH2 minimum high byte.	0xFF
0x58	R/W	TACH3 minimum low byte.	0xFF
0x59	R/W	TACH3 minimum high byte.	0xFF
0x5A	R/W	TACH4 minimum low byte.	0xFF
0x5B	R/W	TACH4 minimum high byte.	0xFF

1. Exceeding any of the TACH limit registers by 1 indicates that the fan is running too slowly or has stalled. The appropriate status bit is set in Interrupt Status Register 2 (0x42) to indicate fan failure. Setting the Configuration Register 1 (0x40) LOCK bit has no effect on these registers.

Table 45. Register 0x55 — TACH1 Minimum High Byte (Power−On Default = 0xFF)

Bit No.	Mnemonic	R/W	Description	
[3:0]	Reserved	Read−only	When Bit 6 of Configuration 2 Register (0x73) is set (single−channel ADC mode), these bits are reserved. Otherwise, these bits represent Bits [3:0] of the TACH1 minimum high byte.	
[7:4]	SCADC	R/W	When Bit 6 of Configuration 2 Register (0x73) is set (single−channel ADC mode), these bits are used to select the only channel from which the ADC will take measurements. Otherwise, these bits represent Bits [7:4] of the TACH1 minimum high byte.	
			Bit Code	**Single−Channel Select**
			0000 0001 0010 0011 0100 0101 0110 0111 1000 1001	+2.5 V_{IN} V_{CCP} V_{CC} +5 V_{IN} +12 V_{IN} Remote 1 temperature Local temperature Remote 2 temperature V_{TT} I_{MON}

Table 46. PWM Configuration Registers

Register Address	R/W (Note 1)	Description	Power−On Default
0x34	R/W	PECI low limit.	0x81
0x5C	R/W	PWM1 configuration.	0x62
0x5D	R/W	PWM2 configuration.	0x62
0x5E	R/W	PWM3 configuration.	0x62

1. These registers become read-only when the Configuration Register 1 (0x40) LOCK bit is set to 1. Any subsequent attempts to write to these registers fail.

Table 47. Register 0x5C, Register 0x5D, and Register 0x5E — PWM1, PWM2, and PWM3 Configuration Registers (Power−On Default = 0x62)

Bit No.	Mnemonic	R/W (Note 1)	Description	
[2:0]	SPIN	R/W	These bits control the startup timeout for PWMx. The PWM output stays high until two valid TACH rising edges are seen from the fan. If there is not a valid TACH signal during the fan TACH measurement directly after the fan startup timeout period, the TACH measurement reads 0xFFFF and Interrupt Status Register 2 reflects the fan fault. If the TACH minimum high and low bytes contain 0xFFFF or 0x0000, then the Interrupt Status Register 2 bit is not set, even if the fan has not started.	
			Bit Code	**Startup Time**
			000 001 010 011 100 101 110 111	No startup timeout 100 ms 250 ms (default) 400 ms 667 ms 1 sec 2 sec 4 sec
[3]	ALT	R/W	Use alternative behavior setting options in Bits [7:5] below for PWMx by setting this bit to 1. Default = 0.	
[4]	INV	R/W	This bit inverts the PWM output. The default is 0, which corresponds to a logic high output for 100% duty cycle. Setting this bit to 1 inverts the PWM output, so a 100% duty cycle corresponds to a logic low output.	
[7:5]	BHVR (Note 2)	R/W	These bits assign each fan to a particular temperature sensor for localized cooling. Setting Bit 3 to Logic 1 in this register chooses whether the default of alternative behavior option is selected.	
			Default Behavior Bits	**Alternative Behavior Bits** (Note 2)
			000 = Remote 1 temperature controls PWMx (automatic fan control mode).	000 = PECI0 reading controls PWMx (automatic fan control mode).
			001 = Local temperature controls PWMx (automatic fan control mode).	001 = PECI1 reading controls PWMx (automatic fan control mode).
			010 = Remote 2 temperature controls PWMx (automatic fan control mode).	010 = PECI2 reading controls PWMx (automatic fan control mode).
			011 = PWMx runs full speed (default).	011 = PECI3 reading controls PWMx (automatic fan control mode).
			100 = PWMx disabled.	100 = Reserved. If selected, fans run at 100% duty cycle.
			101 = Fastest speed calculated by local and Remote 2 temperature controls PWMx.	101 = Fastest of all four PECI channels. Fastest speed calculated by all four PECI readings.
			110 = Fastest speed calculated by all three temperature channel controls PWMx.	110 = Reserved. If selected, fans run at 100% duty cycle.
			111 = Manual mode. PWM duty cycle registers (Register 0x30 to Register 0x32) become writable.	111 = Fastest speed calculated by all of the thermal zones (Local, Remote 1, Remote 2, and PECI temperatures).

1. This register becomes read-only when the Configuration Register 1 (0x40) LOCK bit is set to 1. Any subsequent attempts to write to this register fail.
2. When REPLACE mode is selected, (Register 0x36, Bit 4 set to 1) PWM1 is automatically configured for the alternative behavior setting. Register 0x36, Bits [7:5] should be set to 000 only.

Table 48. Temperature T_{RANGE}/PWM Frequency Registers

Register Address	R/W (Note 1)	Description	Power−On Default
0x5F	R/W	Remote 1 T_{RANGE}/PWM1 frequency.	0xC4
0x60	R/W	Local T_{RANGE}/PWM2 frequency.	0xC4
0x61	R/W	Remote 2 T_{RANGE}/PWM3 frequency.	0xC4

1. These registers become read-only when the Configuration Register 1 (0x40) LOCK bit is set. Any further attempts to write to these registers have no effect.

Table 49. Register 0x5F, Register 0x60, and Register 0x61 — Remote 1 T_{RANGE}/PWM1 Frequency, Local T_{RANGE}/PWM2 Frequency, and Remote 2 T_{RANGE}/PWM3 Frequency (Power−On Default = 0xC4)

Bit No.	Mnemonic	R/W (Note 1)	Description	
[2:0]	FREQ	R/W	These bits control the PWMx frequency (only apply when PWM channel is in low frequency mode).	
			Bit Code	**Frequency**
			000	11.0 Hz
			001	14.7 Hz
			010	22.1 Hz
			011	29.4 Hz
			100	35.3 Hz (default)
			101	44.1 Hz
			110	58.8 Hz
			111	88.2 Hz
[3]	HF/LF	R/W	HF/LF = 1, high frequency PWM mode is enabled for PWMx. HF/LF = 0, low frequency PWM mode is enabled for PWMx.	
[7:4]	RANGE	R/W	These bits determine the PWM duty cycle vs. the temperature range for automatic fan control.	
			Bit Code	**Temperature**
			0000	2°C
			0001	2.5°C
			0010	3.33°C
			0011	4°C
			0100	5°C
			0101	6.67°C
			0110	8°C
			0111	10°C
			1000	13.33°C
			1001	16°C
			1010	20°C
			1011	26.67°C
			1100	32°C (default)
			1101	40°C
			1110	53.33°C
			1111	80°C

1. This register becomes read-only when the Configuration Register 1 (0x40) LOCK bit is set. Any further attempts to write to this register have no effect.

Table 50. Register 0x62 — Enhanced Acoustics Register 1 (Power−On Default = 0x00)

Bit No.	Mnemonic	R/W (Note 1)	Description	
[2:0]	ACOU (Note 2)	R/W	Assuming that PWMx is associated with the Remote 1 temperature channel, these bits define the maximum rate of change of the PWMx output for Remote 1 temperature−related changes. Instead of the fan speed jumping instantaneously to its newly determined speed, it ramps gracefully at the rate determined by these bits. This feature ultimately enhances the acoustics of the fan.	
			When Bit 7 of Configuration Register 6 (0x10) is 0	
			Bit Code	**Time for 0% to 100%**
			000 = 1 001 = 2 010 = 3 011 = 4 100 = 8 101 = 12 110 = 24 111 = 48	37.5 sec 18.8 sec 12.5 sec 7.5 sec 4.7 sec 3.1 sec 1.6 sec 0.8 sec
			When Bit 7 of Configuration Register 6 (0x10) is 1	
			Bit Code	**Time for 0% to 100%**
			000 = 1 001 = 2 010 = 3 011 = 4 100 = 8 101 = 12 110 = 24 111 = 48	52.2 sec 26.1 sec 17.4 sec 10.4 sec 6.5 sec 4.4 sec 2.2 sec 1.1 sec
[3]	EN1	R/W	When this bit is 1, smoothing is enabled on Remote 1 temperature channel.	
[4]	SYNC	R/W	SYNC = 1 synchronizes fan speed measurements on TACH2, TACH3, and TACH4 to PWM3. This allows up to three fans to be driven from PWM3 output and their speeds to be measured. SYNC = 0 synchronizes only TACH3 and TACH4 to PWM3 output.	
[5]	MIN1	R/W	When the ADT7490 is in automatic fan control mode, this bit defines whether PWM1 is off (0% duty cycle) or at PWM1 minimum duty cycle when the controlling temperature is below its T_{MIN} − hysteresis value. 0 = 0% duty cycle below T_{MIN} − hysteresis. 1 = PWM1 minimum duty cycle below T_{MIN} − hysteresis.	
[6]	MIN2	R/W	When the ADT7490 is in automatic fan speed control mode, this bit defines whether PWM2 is off (0% duty cycle) or at PWM2 minimum duty cycle when the controlling temperature is below its T_{MIN} − hysteresis value. 0 = 0% duty cycle below T_{MIN} − hysteresis. 1 = PWM2 minimum duty cycle below T_{MIN} − hysteresis.	
[7]	MIN3	R/W	When the ADT7490 is in automatic fan speed control mode, this bit defines whether PWM3 is off (0% duty cycle) or at PWM3 minimum duty cycle when the controlling temperature is below its T_{MIN} − hysteresis value. 0 = 0% duty cycle below T_{MIN} − hysteresis. 1 = PWM3 minimum duty cycle below T_{MIN} − hysteresis.	

1. This register becomes read-only when the Configuration Register 1 (0x40) LOCK bit is set to 1. Any further attempts to write to this register have no effect.
2. Setting the relevant bit of Configuration Register 6 (0x10, Bits [2:0]) further decreases these ramp rates by a factor of 4.

Table 51. Register 0x63 — Enhanced Acoustics Register 2 (Power−On Default = 0x00)

Bit No.	Mnemonic	R/W (Note 1)	Description	
[2:0]	ACOU2	R/W	Assuming that PWMx is associated with the local temperature channel, these bits define the maximum rate of change of the PWMx output for local temperature−related changes. Instead of the fan speed jumping instantaneously to its newly determined speed, it ramps gracefully at the rate determined by these bits. This feature ultimately enhances the acoustics of the fan.	
			When Bit 7 of Configuration Register 6 (0x10) is 0	
			Bit Code	**Time for 0% to 100%**
			000 = 1 001 = 2 010 = 3 011 = 4 100 = 8 101 = 12 110 = 24 111 = 48	37.5 sec 18.8 sec 12.5 sec 7.5 sec 4.7 sec 3.1 sec 1.6 sec 0.8 sec
			When Bit 7 of Configuration Register 6 (0x10) is 1	
			Bit Code	**Time for 0% to 100%**
			000 = 1 001 = 2 010 = 3 011 = 4 100 = 8 101 = 12 110 = 24 111 = 48	52.2 sec 26.1 sec 17.4 sec 10.4 sec 6.5 sec 4.4 sec 2.2 sec 1.1 sec
[3]	EN2	R/W	When this bit is 1, smoothing is enabled on the local temperature channel.	
[6:4]	ACOU3	R/W	Assuming that PWMx is associated with the Remote 2 temperature channel, these bits define the maximum rate of change of the PWMx output for Remote 2 Temperature related changes. Instead of the fan speed jumping instantaneously to its newly determined speed, it ramps gracefully at the rate determined by these bits. This feature ultimately enhances the acoustics of the fan.	
[7]	EN3	R/W	When this bit is 1, smoothing is enabled on the Remote 2 temperature channel.	

1. This register becomes read-only when the Configuration Register 1 (0x40) LOCK bit is set to 1. Any further attempts to write to this register have no effect.

Table 52. PWM Minimum Duty Cycle Registers

Register Address	R/W (Note 1)	Description	Power−On Default
0x64	R/W	PWM1 minimum duty cycle.	0x80 (50% duty cycle)
0x65	R/W	PWM2 minimum duty cycle.	0x80 (50% duty cycle)
0x66	R/W	PWM3 minimum duty cycle.	0x80 (50% duty cycle)

1. These registers become read-only when the ADT7490 is in automatic fan control mode.

Table 53. Register 0x64, Register 0x65, and Register 0x66 — PWM1, PWM2, and PWM3 Min Duty Cycles (Power−On Default = 0x80)

Register Address	R/W (Note 1)	Description
[7:0]	R/W	These bits define the PWM_{MIN} duty cycle for PWMx. 0x00 = 0% duty cycle (fan off). 0x40 = 25% duty cycle. 0x80 = 50% duty cycle. 0xFF = 100% duty cycle (fan full speed).

1. This register becomes read-only when the Configuration Register 1 (0x40) LOCK bit is set to 1. Any further attempts to write to this register have no effect.

Table 54. T_{MIN} Registers (Note 1)

Register Address	R/W (Note 2)	Description	Power−On Default
0x67	R/W	Remote 1 temperature T_{MIN}.	0x5A (90°C)
0x68	R/W	Local temperature T_{MIN}.	0x5A (90°C)
0x69	R/W	Remote 2 temperature T_{MIN}.	0x5A (90°C)

1. These are the T_{MIN} registers for each temperature channel. When the temperature measured exceeds T_{MIN}, the appropriate fan runs at minimum speed and increases with temperature according to T_{RANGE}.
2. These registers become read-only when the Configuration Register 1 (0x40) LOCK bit is set. Any further attempts to write to these registers have no effect.

Table 55. $\overline{\text{THERM}}$ Limit Registers (Note 1)

Register Address	R/W (Note 2)	Description	Power−On Default
0x6A	R/W	Remote 1 $\overline{\text{THERM}}$ temperature limit.	0x64 (100°C)
0x6B	R/W	Local $\overline{\text{THERM}}$ temperature limit.	0x64 (100°C)
0x6C	R/W	Remote 2 $\overline{\text{THERM}}$ temperature limit.	0x64 (100°C)

1. If any temperature measured exceeds its $\overline{\text{THERM}}$ limit, all PWM outputs drive their fans at 100% duty cycle. This is a fail-safe mechanism incorporated to cool the system in the event of a critical over temperature. It also ensures some level of cooling in the event that software or hardware locks up. If set to 0x80, this feature is disabled. The PWM output remains at 100% until the temperature drops below $\overline{\text{THERM}}$ limit − hysteresis. If the $\overline{\text{THERM}}$ pin is programmed as an output, exceeding these limits by 0.25°C can cause the $\overline{\text{THERM}}$ pin to assert low as an output.
2. These registers become read-only when the Configuration Register 1 (0x40) LOCK bit is set to 1. Any further attempts to write to these registers have no effect.

Table 56. Temperature/T_{MIN} Hysteresis Registers

Register Address	R/W (Note 1)	Description	Power−On Default
0x6D	R/W	Remote 1 and local temperature/T_{MIN} hysteresis.	0x44
0x6E	R/W	PECI and Remote 2 temperature/T_{MIN} hysteresis.	0x44

1. These registers become read-only when the Configuration Register 1(0x40) LOCK bit is set to 1. Any further attempts to write to these registers have no effect.

Table 57. Register 0x6D — Remote 1 and Local Temperature/T_{MIN} Hysteresis (Power−On Default = 0x44)

Bit No. (Note 1)	Mnemonic	R/W (Note 2)	Description
[3:0]	HYSL	R/W	Local temperature hysteresis. 0°C to 15°C of hysteresis can be applied to the Local temperature AFC control loops.
[7:4]	HYSR1	R/W	Remote 1 temperature hysteresis. 0°C to 15°C of hysteresis can be applied to the Remote 1 Temperature AFC control loops.

1. Each 4-bit value controls the amount of temperature hysteresis applied to a particular temperature channel. Once the temperature for that channel falls below its T_{MIN} value, the fan remains running at PWM_{MIN} duty cycle until the temperature = T_{MIN} − hysteresis. Up to 15°C of hysteresis can be assigned to any temperature channel. The hysteresis value chosen also applies to that temperature channel if its $\overline{\text{THERM}}$ limit is exceeded. The PWM output being controlled goes to 100%, if the $\overline{\text{THERM}}$ limit is exceeded and remains at 100% until the temperature drops below $\overline{\text{THERM}}$ − hysteresis. For acoustic reasons, it is recommended that the hysteresis value not be programmed less than 4°C. Setting the hysteresis value lower than 4°C causes the fan to switch on and off regularly when the temperature is close to T_{MIN}.
2. These registers become read-only when the Configuration Register 1 LOCK bit is set to 1. Any further attempts to write to these registers have no effect.

Table 58. Register 0x6E — Remote 2 and PECI Temperature/T_{MIN} Hysteresis (Power−On Default = 0x44)

Bit No. (Note 1)	Mnemonic	R/W (Note 2)	Description
[3:0]	HYSP	R/W	PECI temperature hysteresis. 0°C to 15°C of hysteresis can be applied to the PECI AFC control loops.
[7:4]	HYSR2	R/W	Remote 2 temperature hysteresis. 0°C to 15°C of hysteresis can be applied to the local temperature AFC control loops.

1. Each 4-bit value controls the amount of temperature hysteresis applied to a particular temperature channel. Once the temperature for that channel falls below its T_{MIN} value, the fan remains running at PWM_{MIN} duty cycle until the temperature = T_{MIN} − hysteresis. Up to 15°C of hysteresis can be assigned to any temperature channel. The hysteresis value chosen also applies to that temperature channel, if its $\overline{THERM}$ limit is exceeded. The PWM output being controlled goes to 100%, if the $\overline{THERM}$ limit is exceeded and remains at 100% until the temperature drops below $\overline{THERM}$ − hysteresis. For acoustic reasons, it is recommended that the hysteresis value not be programmed less than 4°C. Setting the hysteresis value lower than 4°C causes the fan to switch on and off regularly when the temperature is close to T_{MIN}.
2. These registers become read-only when the Configuration Register 1 (0x40) LOCK bit is set to 1. Any further attempts to write to these registers have no effect.

Table 59. Register 0x6F — XNOR Tree Test Enable (Power−On Default = 0x00)

Bit No.	Mnemonic	R/W (Note 1)	Description
[0]	XEN	R/W	If the XEN bit is set to 1, the device enters the XNOR tree test mode. Clearing the bit removes the device from the XNOR tree test mode.
[7:1]	RES	R/W	Unused/reserved. Do not write to these bits.

1. This register becomes read-only when the Configuration Register 1 (0x40) LOCK bit is set to 1. Any further attempts to write to this register have no effect.

Table 60. Register 0x70 — Remote 1 Temperature Offset (Power−On Default = 0x00)

Bit No.	R/W (Note 1)	Description
[7:0]	R/W	Allows a temperature offset to be automatically applied to the Remote 1 temperature channel measurement. Bit 1 of Configuration Register 5 (0x7C) determines the range and resolution of this register.

1. This register becomes read-only when the Configuration Register 1 (0x40) LOCK bit is set to 1. Any further attempts to write to this register have no effect.

Table 61. Register 0x71 — Local Temperature Offset (Power−On Default = 0x00)

Bit No.	R/W (Note 1)	Description
[7:0]	R/W	Allows a temperature offset to be automatically applied to the local temperature measurement. Bit 1 of Configuration Register 5 (0x7C) determines the range and resolution of this register.

1. This register becomes read-only when the Configuration Register 1 (0x40) LOCK bit is set to 1. Any further attempts to write to this register have no effect.

Table 62. Register 0x72 — Remote 2 Temperature Offset (Power−On Default = 0x00)

Bit No.	R/W (Note 1)	Description
[7:0]	R/W	Allows a temperature offset to be automatically applied to the Remote 2 temperature channel measurement. Bit 1 of Configuration Register 5 (0x7C) determines the range and resolution of this register.

1. This register becomes read-only when the Configuration Register 1 (0x40) LOCK bit is set to 1. Any further attempts to write to this register have no effect.

Table 63. Register 0x73 — Configuration Register 2 (Power−On Default = 0x00)

Bit No.	Mnemonic	R/W (Note 1)	Description
0	FanPresDT	R/W	When FanPresDT = 1, the state of Bits [3:1] of this register reflects the presence of a 4−wire fan on the appropriate TACH channel.
1	Fan1Detect	Read−only	Fan1Detect = 1 indicates that a 4−wire fan is connected to the PWM1 input.
2	Fan2Detect	Read−only	Fan2Detect = 1 indicates that a 4−wire fan is connected to the PWM2 input.
3	Fan3Detect	Read−only	Fan3Detect = 1 indicates that a 4−wire fan is connected to the PWM3 input.
4	AVG	R/W	AVG = 1 indicates that averaging on the temperature and voltage measurements is turned off. This allows measurements on each channel to be made much faster (x16).
5	ATTN	R/W	ATTN = 1 indicates that the ADT7490 removes the attenuators from the +2.5 V_{IN}, V_{CCP}, +5 V_{IN}, and +12 V_{IN} inputs. These inputs can be used for other functions such as connecting up external sensors. It is also possible to remove attenuators from individual channels using Bits [7:4] of Configuration Register 4 (0x7D).
6	CONV	R/W	CONV = 1 indicates that the ADT7490 is put into a single−channel ADC conversion mode. In this mode, the ADT7490 can be made to read continuously from one input only, for example, Remote 1 temperature. The appropriate ADC channel is selected by writing to Bits [7:4] of TACH1 minimum high byte register (0x55).
			When CONV = 1, Bits [7:4], Register 0x55
			Bit Code / **ADC Channel Selected**
			0000 — +2.5 V_{IN} 0001 — V_{CCP} 0010 — V_{CC} 0011 — +5 V_{IN} 0100 — +12 V_{IN} 0101 — Remote 1 temperature 0110 — Local temperature 0111 — Remote 2 temperature 1000 — V_{TT} 1001 — I_{MON}
7	Shutdown	R/W	When the shutdown bit is set to 1, the ADT7490 goes into shutdown mode.

1. This register becomes read-only when the Configuration Register 1 (0x40) LOCK bit is set to 1. Any further attempts to write to this register have no effect.

Table 64. Register 0x74 — Interrupt Mask Register 1 (Power−On Default = 0x00)

Bit No.	Mnemonic	R/W	Description
[0]	+2.5 V_{IN}/$\overline{THERM}$	R/W	+2.5 V_{IN}/$\overline{THERM}$ = 1 masks $\overline{SMBALERT}$ for out−of−limit conditions on the +2.5 V_{IN}/$\overline{THERM}$ timer channel.
[1]	V_{CCP}	R/W	V_{CCP} = 1 masks $\overline{SMBALERT}$ for out−of−limit conditions on the V_{CCP} channel.
[2]	V_{CC}	R/W	V_{CC} = 1 masks $\overline{SMBALERT}$ for out−of−limit conditions on the V_{CC} channel.
[3]	+5 V_{IN}	R/W	+5 V_{IN} = 1 masks $\overline{SMBALERT}$ for out−of−limit conditions on the +5 V_{IN} channel.
[4]	R1T	R/W	R1T = 1 masks $\overline{SMBALERT}$ for out−of−limit conditions on the Remote 1 temperature channel.
[5]	LT	R/W	LT = 1 masks $\overline{SMBALERT}$ for out−of−limit conditions on the local temperature channel.
[6]	R2T	R/W	R2T = 1 masks $\overline{SMBALERT}$ for out−of−limit conditions on the Remote 2 temperature channel.
[7]	OOL	R/W	OOL = 1 masks $\overline{SMBALERT}$ assertions when the OOL status bit is set. Note that the OOL mask bit is independent of the individual mask bits associated with Interrupt Status Register 2. Therefore, if the intention is to mask $\overline{SMBALERT}$ assertions for any of the Interrupt Status Register 2 bits, OOL must also be masked.

Table 65. Register 0x75 — Interrupt Mask Register 2 (Power−On Default = 0x00)

Bit No.	Mnemonic	R/W	Description
[0]	+12 V_{IN}	R/W	When Pin 21 is configured as a +12 V_{IN} input, +12 V_{IN} = 1 masks $\overline{\text{SMBALERT}}$ for out−of−limit conditions on the +12 V_{IN} channel.
[1]	OOL	R/W	OOL = 1 masks $\overline{\text{SMBALERT}}$ assertions when the OOL status bit is set. Note that the OOL mask bit is independent of the individual mask bits in Interrupt Mask Register 3 (0x82). Therefore, if the intention is to mask $\overline{\text{SMBALERT}}$ assertions for any of the Interrupt Status Register 4 bits, OOL must also be masked.
[2]	FAN1	R/W	FAN1 = 1 masks $\overline{\text{SMBALERT}}$ for a Fan 1 fault.
[3]	FAN2	R/W	FAN2 = 1 masks $\overline{\text{SMBALERT}}$ for a Fan 2 fault.
[4]	FAN3	R/W	FAN3 = 1 masks $\overline{\text{SMBALERT}}$ for a Fan 3 fault.
[5]	Fan4/ $\overline{\text{THERM}}$	R/W	If Pin 14 is configured as TACH4, Fan4/ $\overline{\text{THERM}}$ = 1 masks $\overline{\text{SMBALERT}}$ for a Fan 4 fault. If Pin 14 is configured as $\overline{\text{THERM}}$, Fan4/ $\overline{\text{THERM}}$ = 1 masks $\overline{\text{SMBALERT}}$ for an exceeded $\overline{\text{THERM}}$ timer limit.
[6]	D1 FAULT	R/W	D1 = 1 masks $\overline{\text{SMBALERT}}$ for a diode open or short on a Remote 1 channel.
[7]	D2 FAULT	R/W	D2 = 1 masks $\overline{\text{SMBALERT}}$ for a diode open or short on a Remote 2 channel.

Table 66. Register 0x76 — Extended Resolution Register 1 (Power−On Default = 0x00) (Note 1)

Bit No.	Mnemonic	R/W	Description
[1:0]	+2.5 V_{IN}	Read−only	+2.5 V_{IN} LSBs. Holds the 2 LSBs of the 10−bit +2.5 V_{IN} measurement.
[3:2]	V_{CCP}	Read−only	V_{CCP} LSBs. Holds the 2 LSBs of the 10−bit V_{CCP} measurement.
[5:4]	V_{CC}	Read−only	V_{CC} LSBs. Holds the 2 LSBs of the 10−bit V_{CC} measurement.
[7:6]	+5 V_{IN}	Read−only	+5 V_{IN} LSBs. Holds the 2 LSBs of the 10−bit +5 V_{IN} measurement.

1. If this register is read, this register and the registers holding the MSB of each reading are frozen until read.

Table 67. Register 0x77 — Extended Resolution Register 2 (Power−On Default = 0x00) (Note 1)

Bit No.	Mnemonic	R/W	Description
[1:0]	+12 V_{IN}	Read−only	+12 V_{IN} LSBs. Holds the 2 LSBs of the 10−bit +12 V_{IN} measurement.
[3:2]	TDM1	Read−only	Remote 1 temperature LSBs. Holds the 2 LSBs of the 10−bit Remote 1 temperature measurement.
[5:4]	LTMP	Read−only	Local temperature LSBs. Holds the 2 LSBs of the 10−bit local temperature measurement.
[7:6]	TDM2	Read−only	Remote 2 temperature LSBs. Holds the 2 LSBs of the 10−bit Remote 2 temperature measurement.

1. If this register is read, this register and the registers holding the MSB of each reading are frozen until read.

Table 68. Register 0x78 — Configuration Register 3 (Power−On Default = 0x00)

Bit No.	Mnemonic	R/W (Note 1)	Description
[0]	ALERT Enable	R/W	ALERT = 1, Pin 10 (PWM2/ $\overline{\text{SMBALERT}}$) is configured as an $\overline{\text{SMBALERT}}$ interrupt output to indicate out−of−limit error conditions. ALERT = 0, Pin 10 (PWM2/ $\overline{\text{SMBALERT}}$) is configured as the PWM2 output.
[1]	$\overline{\text{THERM}}$/ +2.5V_{IN}	R/W	$\overline{\text{THERM}}$ = 1 enables $\overline{\text{THERM}}$ functionality on Pin 22 and Pin 14, if Pin 14 is configured as $\overline{\text{THERM}}$, determined by Bit 0 and Bit 1 (Pin 14 Func) of Configuration Register 4 (0x7D). When $\overline{\text{THERM}}$ is asserted, if the fans are running and the BOOST bit is set, then the fans run at full speed. Alternatively, $\overline{\text{THERM}}$ can be programmed so that a timer is triggered to time how long $\overline{\text{THERM}}$ has been asserted. $\overline{\text{THERM}}$ = 0 enables +2.5V_{IN} measurement on Pin 22 and disables $\overline{\text{THERM}}$. If Bits [5:7] of Configuration Register 5 (0x7C) are set, $\overline{\text{THERM}}$ is bidirectional. If they are 0, $\overline{\text{THERM}}$ is a timer input only.

Pin 14 Func (0x7D)	$\overline{\text{THERM}}$/+2.5 V_{IN} (0x78)	Pin 22	Pin 14
00	0	+2.5 V_{IN}	TACH4
01	0	+2.5 V_{IN}	TACH4
10	0	+2.5 V_{IN}	$\overline{\text{SMBALERT}}$
11	0	+2.5 V_{IN}	N/A
00	1	$\overline{\text{THERM}}$	TACH4
01	1	+2.5 V_{IN}	$\overline{\text{THERM}}$
10	1	$\overline{\text{THERM}}$	$\overline{\text{SMBALERT}}$
11	1	$\overline{\text{THERM}}$	N/A

[2]	BOOST	R/W	When $\overline{\text{THERM}}$ is an input and BOOST = 1, assertion of $\overline{\text{THERM}}$ causes all fans to run at the maximum programmed duty cycle for fail−safe cooling.
[3]	FAST	R/W	FAST = 1 enables fast TACH measurements on all channels. This increases the TACH measurement rate from once per second to once every 250 ms (4x).
[4]	DC1	R/W	DC1 = 1 enables TACH measurements to be continuously made on TACH1. Fans must be driven by dc. Setting this bit prevents pulse stretching because it is not required for dc−driven motors.
[5]	DC2	R/W	DC2 = 1 enables TACH measurements to be continuously made on TACH2. Fans must be driven by dc. Setting this bit prevents pulse stretching because it is not required for dc−driven motors.
[6]	DC3	R/W	DC3 = 1 enables TACH measurements to be continuously made on TACH3. Fans must be driven by dc. Setting this bit prevents pulse stretching because it is not required for dc−driven motors.
[7]	DC4	R/W	DC4 = 1 enables TACH measurements to be continuously made on TACH4. Fans must be driven by dc. Setting this bit prevents pulse stretching because it is not required for dc−driven motors.

1. Bits [3:0] of this register become read-only when the Configuration Register 1 LOCK (0x40) bit is set to 1. Any further attempts to write to Bits [3:0] have no effect.

Table 69. Register 0x79 — $\overline{\text{THERM}}$ Timer Status Register (Power−On Default = 0x00)

Bit No.	Mnemonic	R/W	Description
[0]	ASRT/ TMR0	R	This bit is set high on the assertion of the $\overline{\text{THERM}}$ input and is cleared on read. If the $\overline{\text{THERM}}$ assertion time exceeds 45.52 ms, this bit is set and becomes the LSB of the 8−bit TMR reading. This allows $\overline{\text{THERM}}$ assertion times from 45.52 ms to 5.82 sec to be reported back with a resolution of 22.76 ms.
[7:1]	TMR	R	Times how long $\overline{\text{THERM}}$ input is asserted. These seven bits read 0 until the $\overline{\text{THERM}}$ assertion time exceeds 45.52 ms.

Table 70. Register 0x7A — $\overline{\text{THERM}}$ Timer Limit Register (Power−On Default = 0x00)

Bit No.	Mnemonic	R/W	Description
[7:0]	LIMT	R/W	Sets maximum $\overline{\text{THERM}}$ assertion length allowed before an interrupt is generated. This is an 8−bit limit with a resolution of 22.76 ms allowing $\overline{\text{THERM}}$ assertion limits of 45.52 ms to 5.82 sec to be programmed. If the $\overline{\text{THERM}}$ assertion time exceeds this limit, Bit 5 (FAN4/$\overline{\text{THERM}}$) of Interrupt Status Register 2 (0x42) is set. If the limit value is 0x00, an interrupt is generated immediately on the assertion of the $\overline{\text{THERM}}$ input. If $\overline{\text{THERM}}$ is configured as an output, the $\overline{\text{THERM}}$ timer limit should be set to 0xFF to avoid unwanted alerts from being generated.

Table 71. Register 0x7B — TACH Pulses per Revolution Register (Power−On Default = 0x55)

Bit No.	Mnemonic	R/W	Description	
[1:0]	FAN1	R/W	Sets number of pulses to be counted when measuring Fan 1 speed. Can be used to determine fan pulses per revolution for unknown fan type.	
			Bit Code	**Pulses Counted**
			00 01 10 11	1 2 (default) 3 4
[3:2]	FAN2	R/W	Sets number of pulses to be counted when measuring Fan 2 speed. Can be used to determine fan pulses per revolution for unknown fan type.	
			Bit Code	**Pulses Counted**
			00 01 10 11	1 2 (default) 3 4
[5:4]	FAN3	R/W	Sets number of pulses to be counted when measuring Fan 3 speed. Can be used to determine fan pulses per revolution for unknown fan type.	
			Bit Code	**Pulses Counted**
			00 01 10 11	1 2 (default) 3 4
[7:6]	FAN4	R/W	Sets number of pulses to be counted when measuring Fan 4 speed. Can be used to determine fan pulses per revolution for unknown fan type.	
			Bit Code	**Pulses Counted**
			00 01 10 11	1 2 (default) 3 4

Table 72. Register 0x7C — Configuration Register 5 (Power−On Default = 0x01)

Bit No.	Mnemonic	R/W (Note 1)	Description
[0]	TWOS COMPL	R/W	TWOS COMPL = 1 sets the temperature range to the twos complement temperature range. TWOS COMPL = 0 changes the temperature range to the Offset 64 temperature range. When this bit is changed, the ADT7490 interprets all relevant temperature register values as defined by this bit.
[1]	Temp Offset	R/W	Temp Offset = 0 sets offset range to −63°C to +64°C with 0.5°C resolution. Temp Offset = 1 sets offset range to −63°C to +127°C with 1°C resolution. These settings apply to Register 0x70, Register 0x71, and Register 0x72 (Remote 1, Internal, and Remote 2 Temperature offset registers. Note that PECI offset is always 1°C resolution).
[3:2]	RES	R/W	Reserved.
[4]	PECI R1 $\overline{\text{THERM}}$ Output Only	R/W	PECI R1 = 1 enables $\overline{\text{THERM}}$ assertions when the PECI temperature read is higher than the PECI $T_{CONTROL}$ limit and the $\overline{\text{THERM}}$ pin is bidirectional. If $\overline{\text{THERM}}$ is configured as an output, the $\overline{\text{THERM}}$ timer limit register (0x7A) should be set to 0xFF to avoid unwanted alerts from being generated. PECI R1 = 0 indicates that the $\overline{\text{THERM}}$ pin is configured as a timer input only. Can also be disabled by writing one of the following values to the PECI $T_{CONTROL}$ limit register (0x3D): Writing −64°C in Offset 64 mode. Writing −128°C in twos complement mode.
[5]	R1 $\overline{\text{THERM}}$ Output Only	R/W	R1 = 1 enables $\overline{\text{THERM}}$ assertions when the Remote 1 temperature read is higher than the Remote 1 $\overline{\text{THERM}}$ limit and the $\overline{\text{THERM}}$ pin is bidirectional. If $\overline{\text{THERM}}$ is configured as an output, the $\overline{\text{THERM}}$ timer limit (Register 0x7A) should be set to 0xFF to avoid unwanted alerts from being generated.
			R1 = 0 indicates that the $\overline{\text{THERM}}$ pin is configured as a timer input only. Can also be disabled by writing one of the following values to the Remote 1 $\overline{\text{THERM}}$ Temp Limit register (0x6A): Writing −64°C in Offset 64 mode. Writing −128°C in twos complement mode.
[6]	Local $\overline{\text{THERM}}$ Output Only	R/W	R1 = 1 enables $\overline{\text{THERM}}$ assertions when the Local temperature read is higher than the Local $\overline{\text{THERM}}$ limit and the $\overline{\text{THERM}}$ pin is bidirectional. If $\overline{\text{THERM}}$ is configured as an output, the $\overline{\text{THERM}}$ timer limit (Register 0x7A) should be set to 0xFF to avoid unwanted alerts from being generated. R1 = 0 indicates that the $\overline{\text{THERM}}$ pin is configured as a timer input only. Can also be disabled by writing one of the below values to the local $\overline{\text{THERM}}$ limit register (0x6B): Writing −64°C in Offset 64 mode. Writing −128°C in twos complement mode.
[7]	R2 $\overline{\text{THERM}}$ Output Only	R/W	R1 = 1 enables $\overline{\text{THERM}}$ assertions when the Remote 2 temperature read is higher than the Remote 2 $\overline{\text{THERM}}$ limit and the $\overline{\text{THERM}}$ pin is bidirectional. If $\overline{\text{THERM}}$ is configured as an output, the $\overline{\text{THERM}}$ timer limit (Register 0x7A) should be set to 0xFF to avoid unwanted alerts from being generated. R1 = 0 indicates that the $\overline{\text{THERM}}$ pin is configured as a timer input only. C an also be disabled by writing one of the below values to the Remote 2 $\overline{\text{THERM}}$ temperature limit register (0x6C): Writing −64°C in Offset 64 mode. Writing −128°C in twos complement mode.

1. This register becomes read-only when the Configuration Register 1 (0x40) LOCK bit is set to 1. Any further attempts to write to this register have no effect.

Table 73. Register 0x7D — Configuration Register 4 (Power−On Default = 0x00)

Bit No.	Mnemonic	R/W (Note 1)	Description
[1:0]	Pin 14 Func	R/W	These bits set the functionality of Pin 14. 00 = TACH4 (default) 01 = $\overline{\text{THERM}}$ 10 = $\overline{\text{SMBALERT}}$ 11 = Reserved
[2]	$\overline{\text{THERM}}$ Disable	R/W	$\overline{\text{THERM}}$ Disable = 0 enables $\overline{\text{THERM}}$ overtemperature output assuming $\overline{\text{THERM}}$ is correctly configured (0x78, 0x7C, and 0x7D). $\overline{\text{THERM}}$ Disable = 1 disables $\overline{\text{THERM}}$ overtemperature output on all channels. $\overline{\text{THERM}}$ can also be disabled on any channel by: Writing −64°C to the appropriate $\overline{\text{THERM}}$ temperature limit in Offset 64 mode. Writing −128°C to the appropriate $\overline{\text{THERM}}$ temperature limit in twos complement mode.
[3]	Max/Full on $\overline{\text{THERM}}$	R/W	Max/Full on $\overline{\text{THERM}}$ = 0 indicates that fans go to 100% when $\overline{\text{THERM}}$ temperature limit is exceeded. Max/Full on $\overline{\text{THERM}}$ = 1 indicates that fans go to maximum speed (0x38, 0x39, 0x3A) when $\overline{\text{THERM}}$ temperature limit is exceeded.
[4]	BpAtt +2.5 V_{IN}	R/W	Bypass +2.5V_{IN} attenuator. When set, the measurement scale for this channel changes from 0 V (0x00) to 2.25 V (0xFF).
[5]	BpAtt V_{CCP}	R/W	Bypass V_{CCP} attenuator. When set, the measurement scale for this channel changes from 0 V (0x00) to 2.25 V (0xFF).
[6]	BpAtt +5 V_{IN}	R/W	Bypass +5 V_{IN} attenuator. When set, the measurement scale for this channel changes from 0 V (0x00) to 2.25 V (0xFF).
[7]	BpAtt +12 V_{IN}	R/W	Bypass +12 V_{IN} attenuator. When set, the measurement scale for this channel changes from 0 V (0x00) to 2.25 V (0xFF).

1. This register becomes read-only when the Configuration Register 1 (0x40) LOCK bit is set to 1. Any further attempts to write to this register have no effect.

Table 74. Register 0x7E — Manufacturer's Test Register 1 (Power−On Default = 0x00)

Bit No.	Mnemonic	R/W (Note 1)	Description
[7:0]	Reserved	Read−only	Manufacturer's test register. These bits are reserved for manufacturer's test purposes and should not be written to under normal operation.

1. This register becomes read-only when the Configuration Register 1 (0x40) LOCK bit is set to 1. Any further attempts to write to this register have no effect.

Table 75. Register 0x7F — Manufacturer's Test Register 2 (Power−On Default = 0x00)

Bit No.	Mnemonic	R/W (Note 1)	Description
[7:0]	Reserved	Read−only	Manufacturer's test register. These bits are reserved for manufacturer's test purposes and should not be written to under normal operation.

1. This register becomes read-only when the Configuration Register 1 (0x40) LOCK bit is set to 1. Any further attempts to write to this register have no effect.

Table 76. Register 0x80 — GPIO Configuration Register (Power−On Default = 0x00)

Bit No.	Mnemonic	R/W	Description
[1:0]	RES	Reserved	Reserved.
[2]	GPIO2	R/W	If GPIO2 is set to input, this register reflects the state of the pin. If GPIO2 is configured as an output, writing to this register asserts the output high or low depending on the polarity.
[3]	GPIO1	R/W	If GPIO1 is set to input, this register reflects the state of the pin. If GPIO1 is configured as an output, writing to this register asserts the output high or low depending on the polarity.
[4]	GPIO2 POL	R/W	GPIO2 polarity bit. Set to 0 for active low. Set to 1 for active high.
[5]	GPIO1 POL	R/W	GPIO1 polarity bit. Set to 0 for active low. Set to 1 for active high.
[6]	GPIO2 DIR	R/W	GPIO2 direction bit. Set to 1 for GPIO1 to act as an input, set to 0 for GPIO2 to act as an output.
[7]	GPIO1 DIR	R/W	GPIO1 direction bit. Set to 1 for GPIO1 to act as an input, set to 0 for GPIO1 to act as an output.

Table 77. Register 0x81 — Interrupt Status Register 4 (Power−On Default = 0x00)

Bit No.	Mnemonic	R/W	Description
[2:0]	RES	Read−only	Reserved.
[3]	PECI1	Read−only	A Logic 1 indicates that the PECI high or low limit has been exceeded by the PECI value from PECI Client Address 0x31. This bit is cleared on a read of the status register only if the error condition has subsided.
[4]	PECI2	Read−only	A Logic 1 indicates that the PECI high or low limit has been exceeded by the PECI value from PECI Client Address 0x32. This bit is cleared on a read of the status register only if the error condition has subsided.
[5]	PECI3	Read−only	A Logic 1 indicates that the PECI high or low limit has been exceeded by the PECI value from PECI Client Address 0x33. This bit is cleared on a read of the status register only if the error condition has subsided.
[6]	I_{MON}	Read−only	A Logic 1 indicates that the I_{MON} high or low limit has been exceeded. This bit is cleared on a read of the status register only if the error condition has subsided.
[7]	V_{TT}	Read−only	A Logic 1 indicates that the V_{TT} high or low limit has been exceeded. This bit is cleared on a read of the status register only if the error condition has subsided.

Table 78. Register 0x82 — Interrupt Mask Register 3 (Power−On Default = 0x00) (Note 1)

Bit No.	Mnemonic	R/W	Description
[0]	PECI0	R/W	A Logic 1 masks $\overline{\text{SMBALERT}}$ assertions for out−of−limit conditions on PECI0.
[1]	DATA	R/W	A Logic 1 masks $\overline{\text{SMBALERT}}$ assertions for PECI data errors.
[2]	COMM	R/W	A Logic 1 masks $\overline{\text{SMBALERT}}$ assertions for PECI communications errors.
[3]	OVT	R/W	OVT = 1 masks $\overline{\text{SMBALERT}}$ for overtemperature $\overline{\text{THERM}}$ conditions.
[6:4]	RES	R/W	Reserved.
[7]	OOL	R/W	OOL = 1 masks $\overline{\text{SMBALERT}}$ assertions when the OOL status bit is set. Note that the OOL mask bit is independent of the individual mask bits of Interrupt Mask Register 4 (0x83). Therefore, if the intention is to mask $\overline{\text{SMBALERT}}$ assertions for any of the Interrupt Status Register 4 bits, OOL must also be masked.

1. If the mask bits in Register 0x82 are set, it is also necessary to set the OOL mask bit in Register 0x75 to ensure the $\overline{\text{SMBALERT}}$ output is not asserted.

Table 79. Register 0x83 — Interrupt Mask Register 4 (Power−On Default = 0x00) (Note 1)

Bit No.	Mnemonic	R/W	Description
[2:0]	RES	R/W	Reserved.
[3]	PECI1	R/W	A Logic 1 masks $\overline{\text{ALERT}}$ assertions for out−of−limit conditions on PECI1.
[4]	PECI2	R/W	A Logic 1 masks $\overline{\text{ALERT}}$ assertions for out−of−limit conditions on PECI2.
[5]	PECI3	R/W	A Logic 1 masks $\overline{\text{ALERT}}$ assertions for out−of−limit conditions on PECI3.
[6]	I_{MON}	R/W	A Logic 1 masks $\overline{\text{ALERT}}$ assertions for out−of−limit conditions on I_{MON}.
[7]	V_{TT}	R/W	A Logic 1 masks $\overline{\text{ALERT}}$ assertions for out−of−limit conditions on V_{TT}.

1. If the mask bits in Register 0x83 are set, it is also necessary to set the OOL mask bit in Register 0x82 to ensure the $\overline{\text{SMBALERT}}$ output is not asserted.

Table 80. V_{TT}, I_{MON} Limit Registers

Register Address	R/W (Note 1)	Description	Power−On Default
0x84	R/W	V_{TT} low limit	0x00
0x85	R/W	I_{MON} low limit	0x00
0x86	R/W	V_{TT} high limit	0xFF
0x87	R/W	I_{MON} high limit	0xFF

1. These registers becomes read-only when the Configuration Register 1 (0x40) LOCK bit is set to 1. Any subsequent attempts to write to these registers fail.

Table 81. Register 0x88 — PECI Configuration Register 2 (Power−On Default = 0x00)

Bit No.	Mnemonic	R/W (Note 1)	Description
[2:0]	RES	R/W	Reserved.
[3]	DOM3	R/W	CPU domain count information. Set to 0 indicates that CPU 4 associated with the PECI3 reading has a single domain (default). Set to 1 indicates that the system CPU4 contains two domains.
[4]	DOM2	R/W	CPU domain count information. Set to 0 indicates that CPU 3 associated with the PECI2 reading has a single domain (default). Set to 1 indicates that the system CPU3 contains two domains.
[5]	DOM1	R/W	CPU domain count information. Set to 0 indicates that CPU 2 associated with the PECI1 reading has a single domain (default). Set to 1 indicates that the system CPU2 contains two domains.
[7:6]	#CPU	R/W	CPU count. These bits indicate the number of CPUs in the system, which provide PECI thermal information to the ADT7490. 00 = 1 CPU (default); indicates that PECI0 data is available from CPU 1 at Address 0x30. 01 = 2 CPUs; indicates that PECI0 data is available from CPU1 at Address 0x30 and PECI1 data is available from CPU 2 at Address 0x31. 10 = 3 CPUs; indicates that PECI0 data is available from CPU1 at Address 0x30, PECI1 data is available from CPU 2 at Address 0x31 and PECI2 data is available from CPU 3 at Address 0x32. 11 = 4 CPUs; indicates that PECI0 data is available from CPU1 at Address 0x30, PECI1 data is available from CPU 2 at Address 0x31, PECI2 data is available from CPU 3 at Address 0x32 and PECI3 data is available from CPU 4 at Address 0x33.

1. This register becomes read-only when the Configuration Register 1 (0x40) LOCK bit is set to 1. Any subsequent attempts to write to this register fail.

Table 82. Operating Point Registers (Note 1 and 2)

Register Address	R/W (Note 3)	Description	Power−On Default
0x8A	R/W	PECI operating point register.	0xFB
0x8B	R/W	Remote 1 operating point register (default = 100°C).	0x64
0x8C	R/W	Local temperature operating point register (default = 100°C).	0x64
0x8D	R/W	Remote 2 operating point register (default = 100°C).	0x64

1. These registers set the target operating point for each temperature channel when the dynamic T_{MIN} control feature is enabled.
2. The fans being controlled are adjusted to maintain temperature about an operating point.
3. This register becomes read-only when the Configuration Register 1 (0x40) LOCK bit is set to 1. Any subsequent attempts to write to this register fail.

Table 83. Register 0x8E — Dynamic T_{MIN} Control Register 1 (Power−On Default = 0x00)

Bit No.	Mnemonic	R/W (Note 1)	Description
[0]	CYR2	R/W	MSB of 3−bit Remote 2 Cycle Value. The other two bits of the code reside in Dynamic T_{MIN} Control Register 2 (0x8F). These three bits define the delay time between making subsequent T_{MIN} adjustments in the control loop in terms of the number of monitoring cycles. The system has associated thermal time constants that need to be found to optimize the response of fans and the control loop.
[1]	V_{CCP}LO	R/W	V_{CCP}LO = 1. When the power is supplied from 3.3 V STANDBY and the core voltage (V_{CCP}) drops below its V_{CCP} low limit value (0x46), the following occurs: Status Bit 1 in Status Register 1 is set. $\overline{\text{SMBALERT}}$ is generated, if enabled. $\overline{\text{PROCHOT}}$ monitoring is disabled. Dynamic T_{MIN} control is disabled. The device is prevented from entering shutdown. Everything is re−enabled once V_{CCP} increases above the V_{CCP} low limit.
[2]	PHTR1	R/W	PHTR1 = 1 copies the Remote 1 current temperature to the Remote 1 operating point register if $\overline{\text{THERM}}$ is asserted. The operating point contains the temperature at which $\overline{\text{THERM}}$ is asserted, allowing the system to run as quietly as possible without affecting system performance. PHTR1 = 0 ignores any $\overline{\text{THERM}}$ assertions on the $\overline{\text{THERM}}$ pin. The Remote 1 operating point register reflects its programmed value.
[3]	PHTL	R/W	PHTL = 1 copies the local channel's current temperature to the local operating point register if $\overline{\text{THERM}}$ is asserted. The operating point contains the temperature at which $\overline{\text{THERM}}$ is asserted. This allows the system to run as quietly as possible without affecting system performance. PHTL = 0 ignores any $\overline{\text{THERM}}$ assertions on the $\overline{\text{THERM}}$ pin. The local temperature operating point register reflects its programmed value.
[4]	PHTR2	R/W	PHTR2 = 1 copies the Remote 2 current temperature to the Remote 2 operating point register if $\overline{\text{THERM}}$ is asserted. The operating point contains the temperature at which $\overline{\text{THERM}}$ is asserted, allowing the system to run as quietly as possible without affecting system performance. PHTR2 = 0 ignores any $\overline{\text{THERM}}$ assertions on the $\overline{\text{THERM}}$ pin. The Remote 2 operating point register reflects its programmed value.
[5]	R1T	R/W	R1T = 1 enables dynamic T_{MIN} control on the Remote 1 temperature channel. The chosen T_{MIN} value is dynamically adjusted based on the current temperature, operating point, and high and low limits for this zone. R1T = 0 disables dynamic T_{MIN} control. The T_{MIN} value chosen is not adjusted, and the channel behaves as described in the section.
[6]	LT	R/W	LT = 1 enables dynamic T_{MIN} control on the local temperature channel. The chosen T_{MIN} value is dynamically adjusted based on the current temperature, operating point, and high and low limits for this zone. LT = 0 disables dynamic T_{MIN} control. The T_{MIN} value chosen is not adjusted, and the channel behaves as described in the Automatic Fan Control Overview section.
[7]	R2T	R/W	R2T = 1 enables dynamic T_{MIN} control on the Remote 2 temperature channel. The chosen T_{MIN} value is dynamically adjusted based on the current temperature, operating point, and high and low limits for this zone. R2T = 0 disables dynamic T_{MIN} control. The T_{MIN} value chosen is not adjusted, and the channel behaves as described in the Automatic Fan Control Overview section.

1. This register becomes read-only when the Configuration Register 1 (0x40) LOCK bit is set to 1. Any subsequent attempts to write to this register fail.

Table 84. Register 0x8F — Dynamic T_{MIN} Control Register 2 (Power−On Default = 0x00)

Bit No.	Mnemonic	R/W (Note 1)	Description		
[2:0]	CYR1	R/W	3−Bit Remote 1 Cycle Value. These three bits define the delay time between making subsequent T_{MIN} adjustments in the control loop for the Remote 1 channel in terms of number of monitoring cycles. The system has associated thermal time constants that need to be found to optimize the response of fans and the control loop.		
			Bit Code	**Decrease Cycle**	**Increase Cycle**
			000 001 010 011 100 101 110 111	8 cycles (1 sec) 16 cycles (2 sec) 32 cycles (4 sec) 64 cycles (8 sec) 128 cycles (16 sec) 256 cycles (32 sec) 512 cycles (64 sec) 1024 cycles (128 sec)	16 cycles (2 sec) 32 cycles (4 sec) 64 cycles (8 sec) 128 cycles (16 sec) 256 cycles (32 sec) 512 cycles (64 sec) 1024 cycles (128 sec) 2048 cycles (256 sec)
[5:3]	CYL	R/W	3−Bit Local Temperature Cycle Value. These three bits define the delay time between making subsequent T_{MIN} adjustments in the control loop for the local temperature channel in terms of number of monitoring cycles. The system has associated thermal time constants that need to be found to optimize the response of fans and the control loop.		
			Bit Code	**Decrease Cycle**	**Increase Cycle**
			000 001 010 011 100 101 110 111	8 cycles (1 sec) 16 cycles (2 sec) 32 cycles (4 sec) 64 cycles (8 sec) 128 cycles (16 sec) 256 cycles (32 sec) 512 cycles (64 sec) 1024 cycles (128 sec)	16 cycles (2 sec) 32 cycles (4 sec) 64 cycles (8 sec) 128 cycles (16 sec) 256 cycles (32 sec) 512 cycles (64 sec) 1024 cycles (128 sec) 2048 cycles (256 sec)
[7:6]	CYR2	R/W	2 LSBs of 3−Bit Remote 2 Cycle Value. The MSB of the 3−bit code resides in the Dynamic T_{MIN} Control Register 1 (Register 0x8E). These three bits define the delay time between making subsequent T_{MIN} adjustments in the control loop for the Remote 2 channel in terms of number of monitoring cycles. The system has associated thermal time constants that need to be found to optimize the response of fans and the control loop.		
			Bit Code	**Decrease Cycle**	**Increase Cycle**
			000 001 010 011 100 101 110 111	8 cycles (1 sec) 16 cycles (2 sec) 32 cycles (4 sec) 64 cycles (8 sec) 128 cycles (16 sec) 256 cycles (32 sec) 512 cycles (64 sec) 1024 cycles (128 sec)	16 cycles (2 sec) 32 cycles (4 sec) 64 cycles (8 sec) 128 cycles (16 sec) 256 cycles (32 sec) 512 cycles (64 sec) 1024 cycles (128 sec) 2048 cycles (256 sec)

1. This register becomes read-only when the Configuration Register 1 (0x40) LOCK bit is set to 1. Any subsequent attempts to write to this register fail.

Table 85. Register 0x90 — Dynamic T_{MIN} Control Register 3 (Power−On Default = 0x00)

Bit No.	Mnemonic	R/W (Note 1)	Description		
[2:0]	RES	Reserved	Reserved		
[5:3]	CYP	R/W	3−Bit PECI Temperature Cycle Value. These three bits define the delay time between making subsequent T_{MIN} adjustments in the control loop for the PECI temperature channels in terms of number of monitoring cycles. The system has associated thermal time constants that need to be found to optimize the response of fans and the control loop.		
			Bit Code	**Decrease Cycle**	**Increase Cycle**
			000 001 010 011 100 101 110 111	8 cycles (1 sec) 16 cycles (2 sec) 32 cycles (4 sec) 64 cycles (8 sec) 128 cycles (16 sec) 256 cycles (32 sec) 512 cycles (64 sec) 1024 cycles (128 sec)	16 cycles (2 sec) 32 cycles (4 sec) 64 cycles (8 sec) 128 cycles (16 sec) 256 cycles (32 sec) 512 cycles (64 sec) 1024 cycles (128 sec) 2048 cycles (256 sec)
[6]	PHTP	R/W	PHTR1 = 1 copies the PECI0 current reading to the PECI operating point register if $\overline{\text{THERM}}$ is asserted. The operating point contains the temperature at which $\overline{\text{THERM}}$ is asserted, allowing the system to run as quietly as possible without affecting system performance. PHTR1 = 0 ignores any $\overline{\text{THERM}}$ assertions on the $\overline{\text{THERM}}$ pin. The PECI operating point register reflects its programmed value.		
[7]	PECI	R/W	PECI = 1 enables dynamic T_{MIN} control on the PECI temperature channel. The chosen T_{MIN} value is dynamically adjusted based on the current temperature, operating point, and high and low limits for this zone. PECI = 0 disables dynamic T_{MIN} control. The T_{MIN} value chosen is not adjusted and the channel behaves as described in the Automatic Fan Control Overview section.		

1. This register becomes read-only when the Configuration Register 1 (0x40) LOCK bit is set to 1. Any subsequent attempts to write to this register fail.

Table 86. Register 0x94 — PECI0 Temperature Offset (Power−On Default = 0x00)

Bit No.	R/W (Note 1)	Description
[7:0]	R/W	Allows a temperature offset to be automatically applied to the PECI0 channel measurements. The programmable offset range is from −63°C to +127°C with 1°C resolution.

1. This register becomes read-only when the Configuration Register 1 (0x40) LOCK bit is set to 1. Any further attempts to write to this register have no effect.

Table 87. Register 0x95 — PECI1 Temperature Offset (Power−On Default = 0x00)

Bit No.	R/W (Note 1)	Description
[7:0]	R/W	Allows a temperature offset to be automatically applied to the PECI1 channel measurements. The programmable offset range is from −63°C to +127°C with 1°C resolution.

1. This register becomes read-only when the Configuration Register 1 (0x40) LOCK bit is set to 1. Any further attempts to write to this register have no effect.

Table 88. Register 0x96 — PECI2 Temperature Offset (Power−On Default = 0x00)

Bit No.	R/W (Note 1)	Description
[7:0]	R/W	Allows a temperature offset to be automatically applied to the PECI2 channel measurements. The programmable offset range is from −63°C to +127°C with 1°C resolution.

1. This register becomes read-only when the Configuration Register 1 (0x40) LOCK bit is set to 1. Any further attempts to write to this register have no effect.

Table 89. Register 0x97 — PECI3 Temperature Offset (Power−On Default = 0x00)

Bit No.	R/W (Note 1)	Description
[7:0]	R/W	Allows a temperature offset to be automatically applied to the PECI3 channel measurements. The programmable offset range is from −63°C to +127°C with 1°C resolution.

1. This register becomes read-only when the Configuration Register 1 (0x40) LOCK bit is set to 1. Any further attempts to write to this register have no effect.

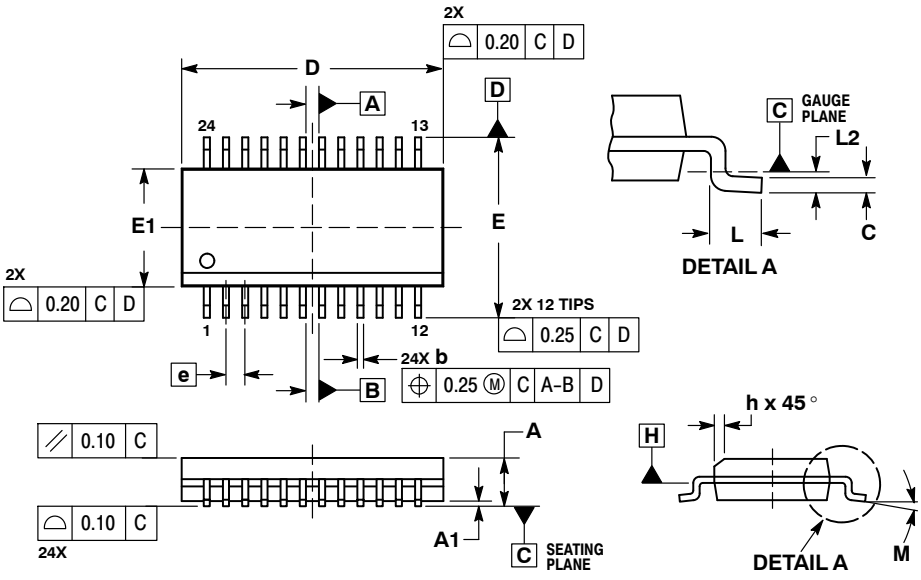
ORDERING INFORMATION

Device Order Number*	Package Type	Package Option	Shipping†
ADT7490ARQZ	24-Lead QSOP	RQ−24	56 Tube
ADT7490ARQZ-REEL			2500 Tape & Reel
ADT7490ARQZ-R7			1000 Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.
*These are Pb−Free packages.

PACKAGE DIMENSIONS

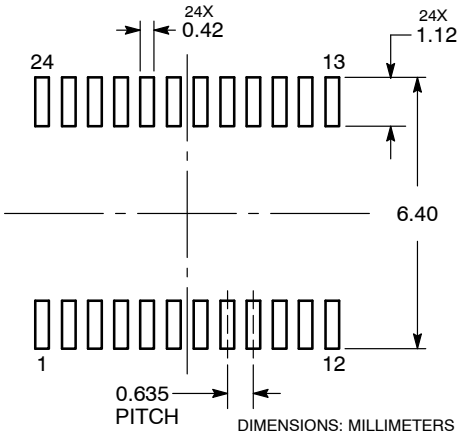
QSOP24 NB
CASE 492B−01
ISSUE A



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION.
4. DIMENSION D DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.15 PER SIDE. DIMENSION E1 DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.15 PER SIDE. D AND E1 ARE DETERMINED AT DATUM H.
5. DATUMS A AND B ARE DETERMINED AT DATUM H.

	MILLIMETERS	
DIM	MIN	MAX
A	1.35	1.75
A1	0.10	0.25
b	0.20	0.30
C	0.19	0.25
D	8.65 BSC	
E	6.00 BSC	
E1	3.90 BSC	
e	0.635 BSC	
h	0.22	0.50
L	0.40	1.27
L2	0.25 BSC	
M	0 °	8 °

SOLDERING FOOTPRINT*



*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

PUBLICATION ORDERING INFORMATION

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